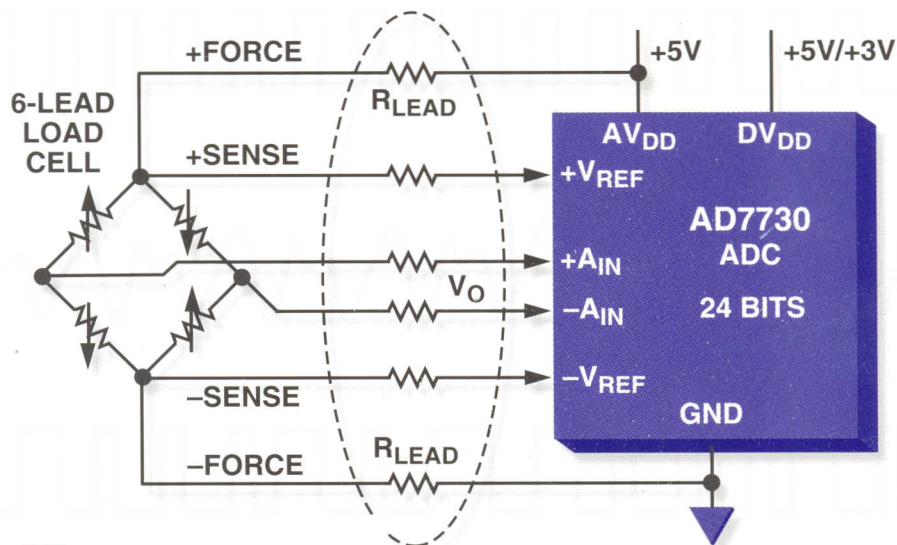
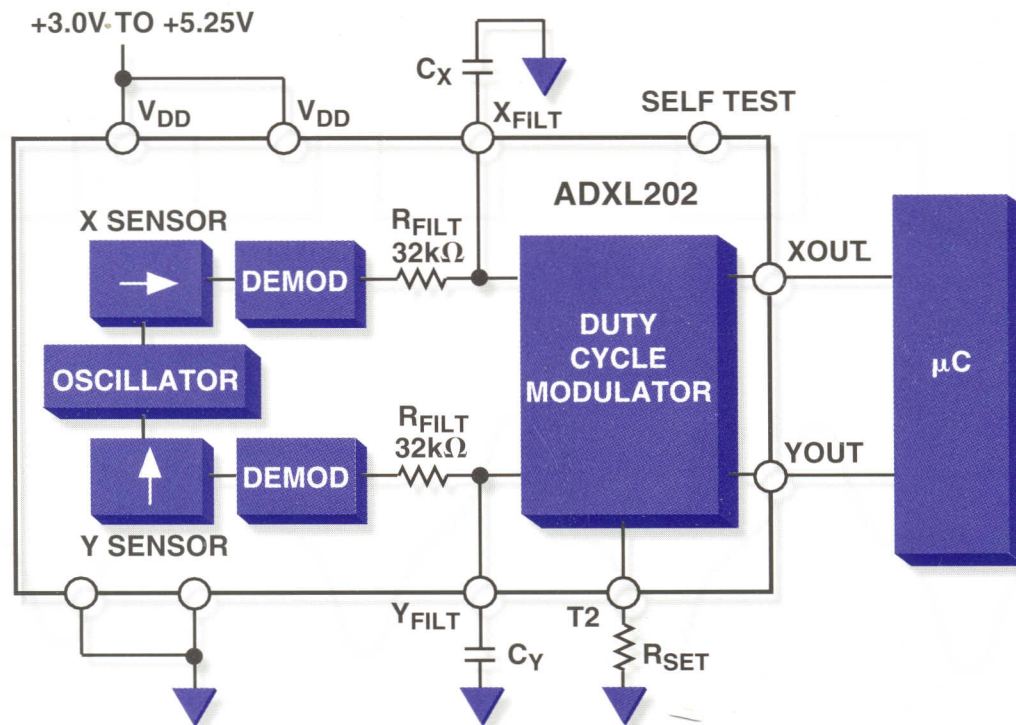


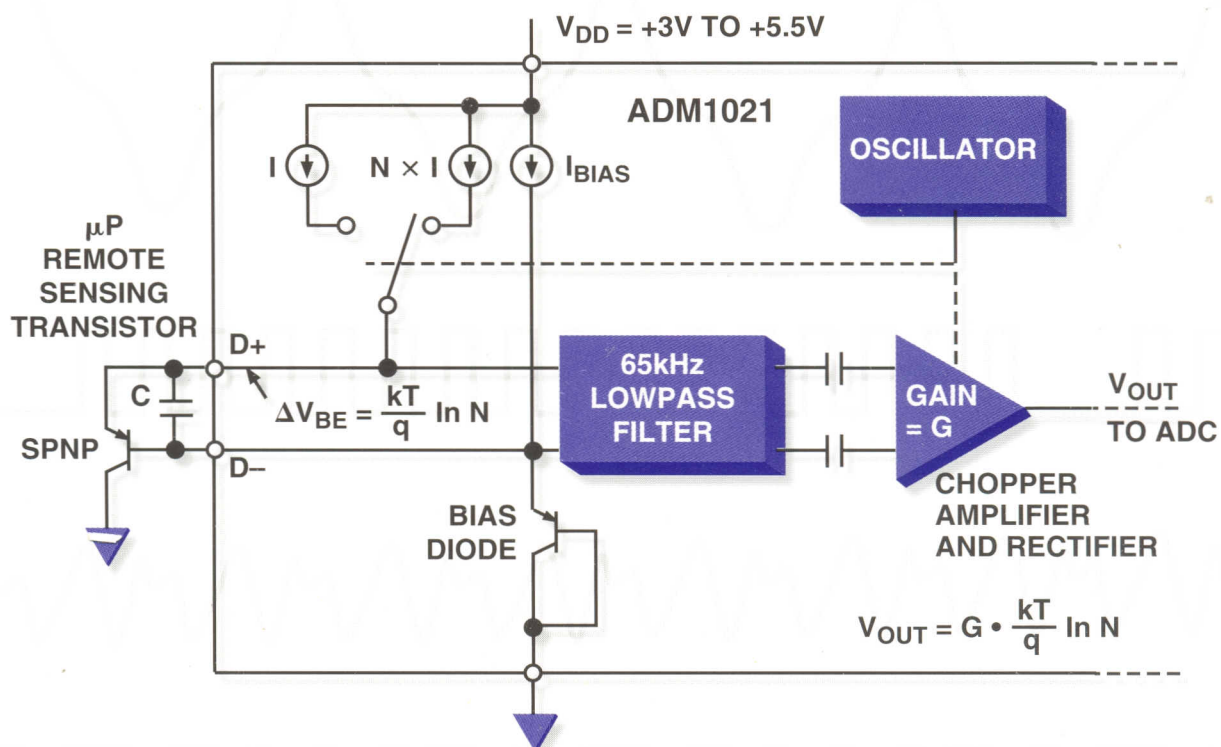
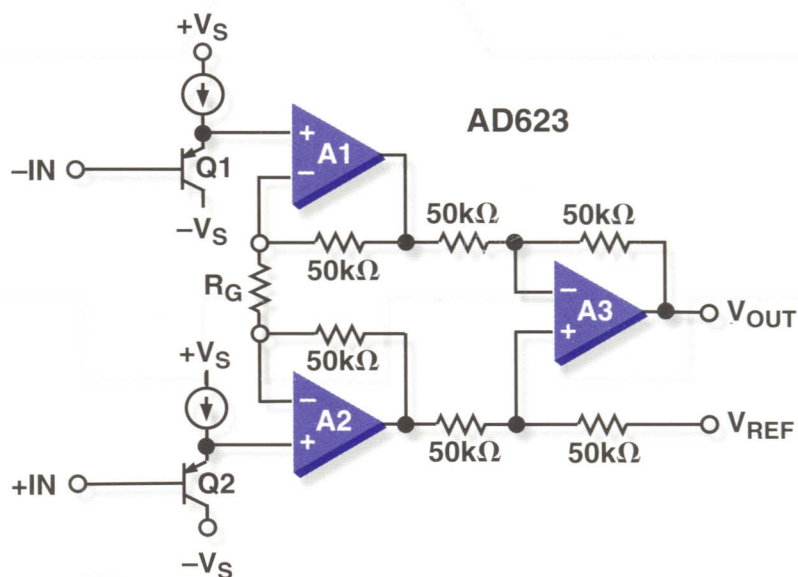
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SECTION 1 AMPLIFIERS

High Speed Current Feedback

High Speed Voltage Feedback

Precision, Low Power

High Speed Comparators

Instrumentation Amplifiers



SECTION 1 AMPLIFIERS

High Speed Current Feedback
High Speed Voltage Feedback
Precision, Low Power
High Speed Comparators
Instrumentation Amplifiers



High Speed Current Feedback Amplifiers

High Speed Current Feedback

Differential Line Driver



AD8014

400 MHz, Low Cost Amplifier

The AD8014 is a revolutionary new current feedback amplifier from Analog Devices. It uses a proprietary circuit architecture to achieve the highest levels of performance at the lowest power.

- 400 MHz Bandwidth
- 4,000 V/us Slew Rate
- 50 ns Overload Recovery
- Fast Settling Time of 24 ns
- Very Low Noise : 3.5 nV/Hz and 5 pA/Hz @ 10 kHz
- Low Distortion : - 70 dB THD @ 5 MHz
- Excellent DC Performance :
 - 5 mV max, 10 μ V/deg C
 - 15 μ A Bias Current
- Operates from 4.5V to 12V Supplies
- Only 1.15 mA max Supply Current
- SOIC-8 and SOT-23-5 Packages

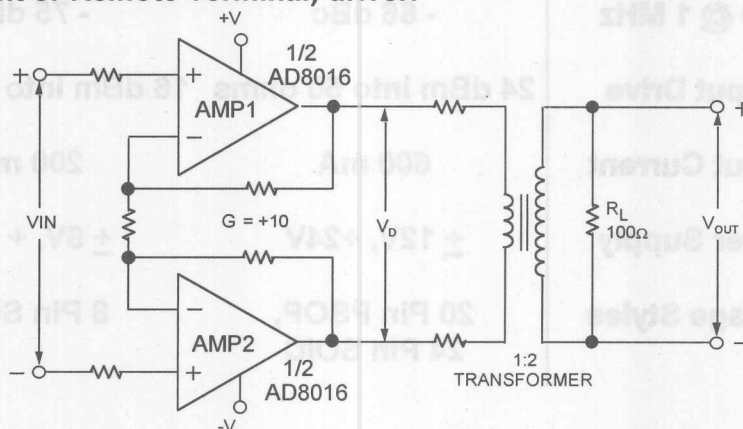
1-4



* Preliminary

AD8016* and AD8017 Low Cost Differential Line Drivers

The AD8016 and AD8017 are high current output, differential line drivers designed for ADSL, HDSL or VDSL subscriber line interfacing. The AD8016 is a next generation version of our popular AD815, and is designed as the “downstream” or CO (Central Office) driver, while the AD8017 is optimized for the “upstream” or CPE (Customer Premises Equipment or Remote Terminal) driver.



1-6

**AD8016 and AD8017 : Key Specs and Features**

Key Spec/Feature	AD8016	AD8017
Bandwidth	350 MHz	220 MHz
Slew Rate	900V/us	4500V/us
THD @ 1 MHz	- 66 dBc	- 75 dBc
Output Drive	24 dBm into 50 ohms	16 dBm into 50 ohms
Output Current	600 mA	200 mA
Power Supply	$\pm 12V$, +24V	$\pm 6V$, + 12V
Package Styles	20 Pin PSOP, 24 Pin SOIC	8 Pin SOIC

1-6



High Speed Voltage Feedback Amplifiers

High Speed Amplifiers
Differential Input/Output
Differential Line Drivers
Rail-Rail Amplifiers



AD8057 & AD8058 375 MHz, Low Cost High Speed Amplifiers

The AD8057 (single) and AD8058 (dual) are next generation AD8055/6 that work on single 5V supplies

- 1150V/us Slew Rate
- Excellent Video Specifications :
 - 0.1 dB Gain Flatness to 28 MHz
 - 0.01%/0.01 deg Differential Gain/Phase Error
- Total Harmonic Distortion :
 - -85 dBc @ 5MHz, - 62 dBc @ 20 MHz
- Input Voltage Noise : 7nV/root Hz @ 100 kHz
- Single + 5V Supply
- 5.4 mA Supply Current per Amplifier
- Package Styles :
 - AD8057 : 8 Pin SOIC and 5 Pin SOT-23
 - AD8058 : 8 Pin SOIC and μ SOIC
- - 40 deg C to + 85 deg C Operating Range

1-8



*** Preliminary**

AD8022* **Dual High Speed, Low Noise Amplifier**

The AD8022 is performance-optimized for use in ADSL, VDSL or proprietary XDSL transceiver designs

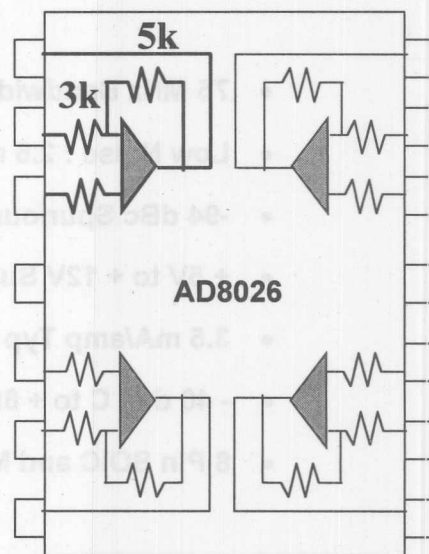
- 75 MHz Bandwidth, $G = +2$
- Low Noise : 2.5 nV/Hz @ 10 kHz
- -94 dBc Spurious-Free Dynamic Range @ 1 MHz
- + 5V to + 12V Supply Operation
- 3.5 mA/amp Typ Supply Current
- - 40 deg C to + 85 deg C Operation
- 8 Pin SOIC and MicroSOIC Packages



AD8026 High Speed Quad Amplifier

The AD8026 provides a precision fixed gain required for driving LCD displays.

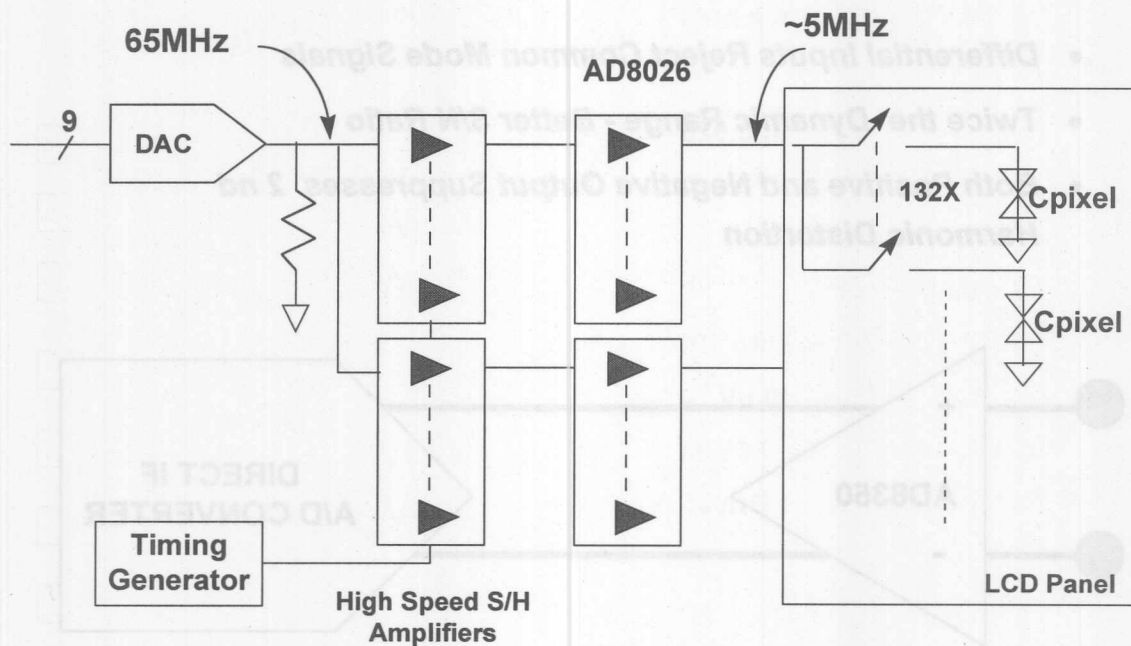
- Precision Fixed Gain: 0.025% Accuracy
- Gain Adjusted with External Resistors
- 120 MHz Bandwidth
- 135 V/us Slew Rate
- Fast Settling : 75ns into 100pF load
- Low Input Offset: 500 μ V
- High Voltage Drive: 0.5V to 11.5V
- High Output Current Drive: 50mA
- +12V Supply
- 14 Pin SOIC Package



1-10



LCD Display Signal Chain

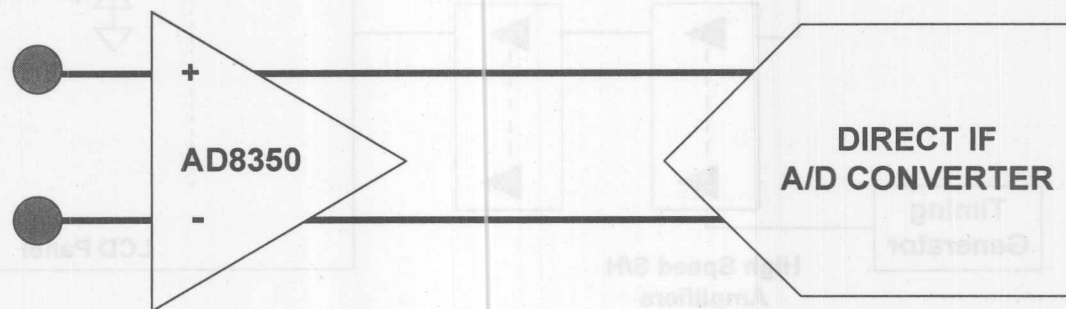


1-11



Why Differential at High Frequencies?

- *Differential Inputs Reject Common Mode Signals*
- *Twice the Dynamic Range - Better S/N Ratio*
- *Both Positive and Negative Output Suppresses 2nd Harmonic Distortion*



1 - 12

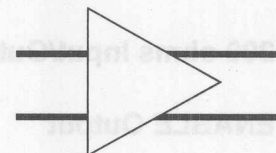


* Preliminary

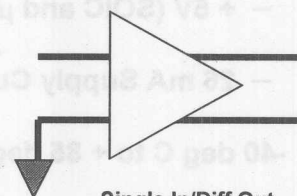
AD8350*

1.2 GHz Low Distortion Differential RF/IF Amplifier

- Three Gain Versions :
 - AD8350-10 : 10 dB
 - AD8350-15 : 15 dB
 - AD8350-20 : 20 dB
- Flat Response to 600 MHz
- 3rd Order Intermodulation Distortion¹ :
 - - 67 dBc
 - - 83 dBc @ 50 MHz
- 3rd Order Intercept (IP3)¹ : + 32 dBm
- Low Noise Figure¹ : 4.9 dB



Diff In/Diff Out



Single In/Diff Out

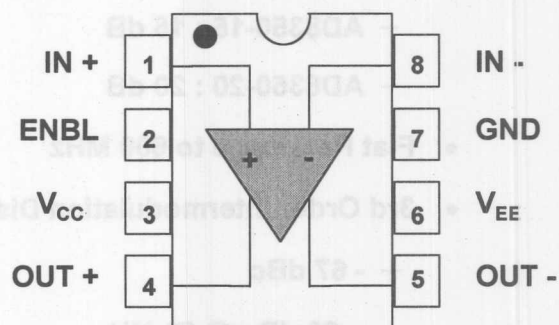
Note 1 : Specs @ 250 MHz

1 - 13



AD8350 (con't)

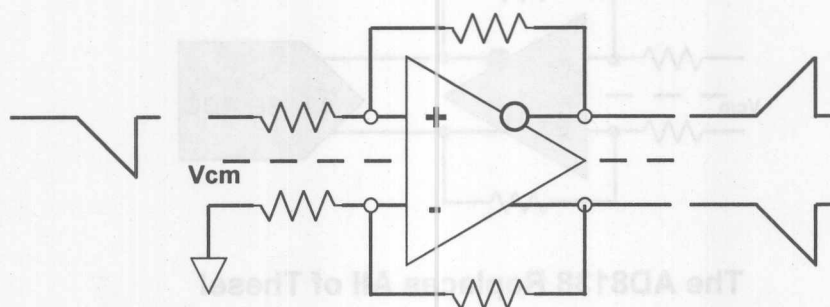
- 200 ohms Input/Output Impedance
- ENABLE Output
- Single/Dual Supply Operation:
 - $\pm 5V$, $+10V$ (SOIC, only)
 - $+ 5V$ (SOIC and μ SOIC)
 - 26 mA Supply Current
- -40 deg C to $+ 85\text{ deg C}$ Operation
- 8 Pin SOIC and μ SOIC Packages



1-14



AD8138 500 MHz Differential I/O Amplifier

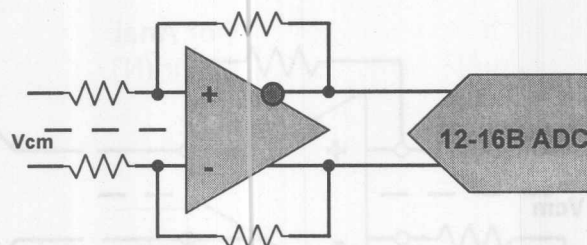


- Spurious-Free Dynamic Range : -92dBc @ 20MHz
- Fast Settling Time : 5ns to 0.01%
- Slew Rate : 1300V/ μ s
- Overdrive Recovery : < 20ns (No Clamp Required)

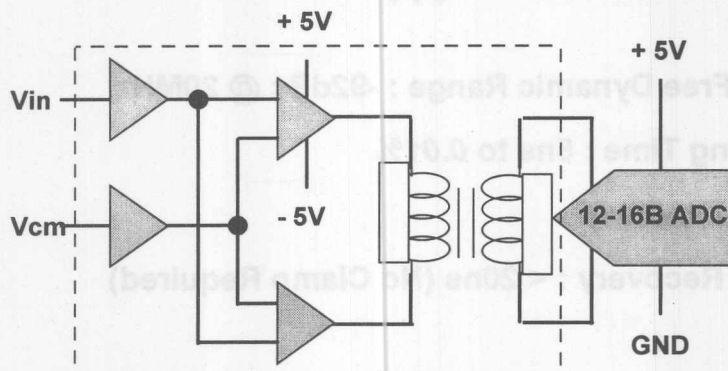
1-15



Compare the AD8138 to a Discrete Solution...



The AD8138 Replaces All of These!



1-16



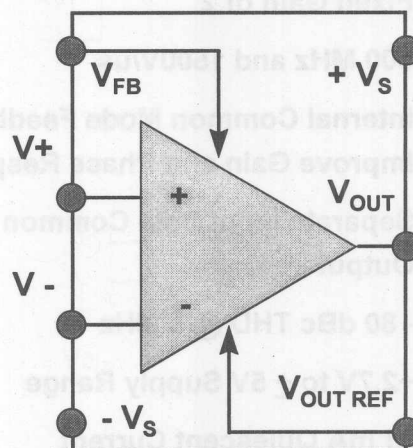
*** Preliminary**

AD8130*/AD8131* Low Cost Differential Driver and Receiver

The AD8130 and AD8131 are designed for Analog and Digital Video Signal Distribution Over Twisted Pair (NTSC to SMPTE259)

AD8130 Receiver :

- Differential Input to Single Ended Output
- User Adjustable Gain
- 350 MHz and 2000V/us
- - 68 dBc THD @ 5 MHz
- - 80 dB CMRR @ 10 MHz
- + 4V to ± 12 V Supply Range
- 7.5 mA Supply Current

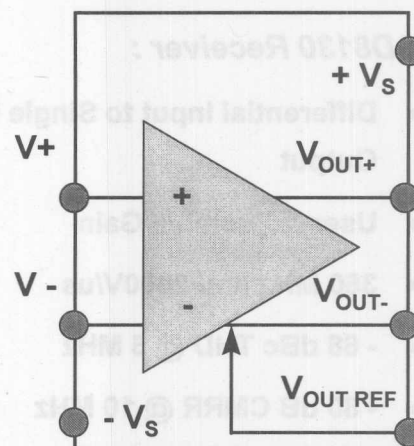




AD8130 and AD8131 Key Specs and Features

AD8131 Driver :

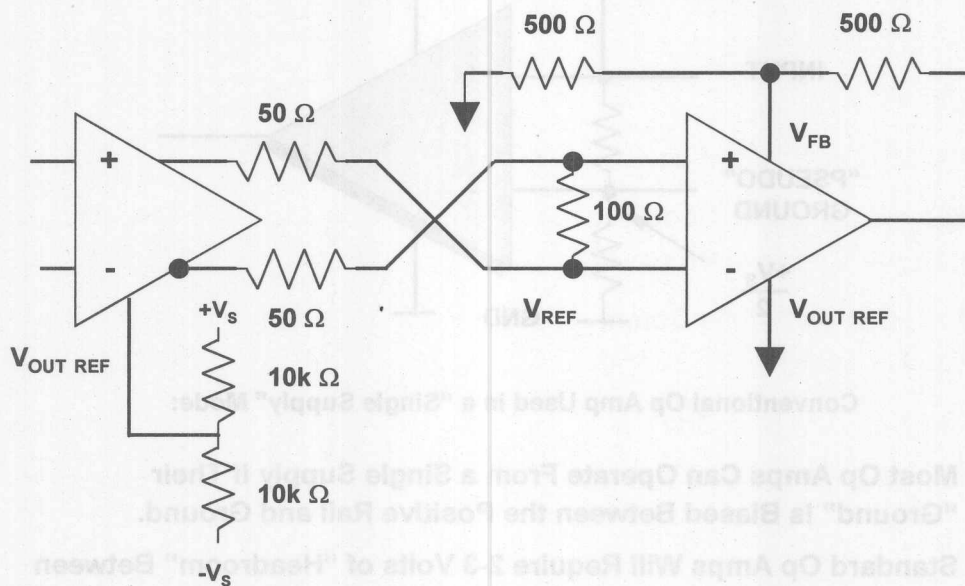
- Differential or Single Ended Input to Differential Output
- Fixed Gain of 2
- 300 MHz and 1500V/us
- Internal Common Mode Feedback to Improve Gain and Phase Response
- Separate Input Sets Common Mode Output Voltage
- - 80 dBc THD @ 5 MHz
- +2.7V to ± 5 V Supply Range
- 11 mA Quiescent Current



1 - 18



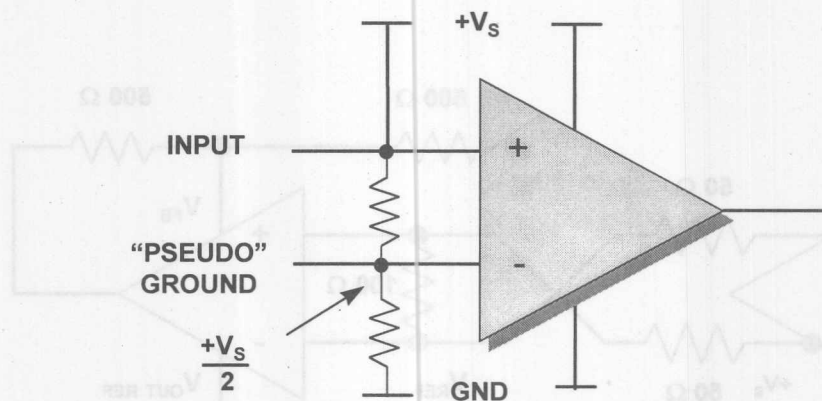
AD8130 and AD8131 Application Example



1-19



What is a Rail-Rail Amplifier?



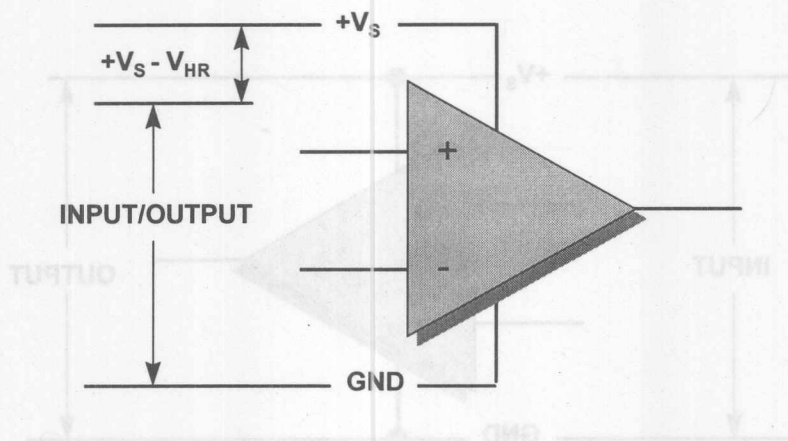
Conventional Op Amp Used in a "Single Supply" Mode:

- Most Op Amps Can Operate From a Single Supply If Their "Ground" Is Biased Between the Positive Rail and Ground.
- Standard Op Amps Will Require 2-3 Volts of "Headroom" Between Supply Rails.

1 - 20



What is a Rail-Rail Amplifier ? (con't)



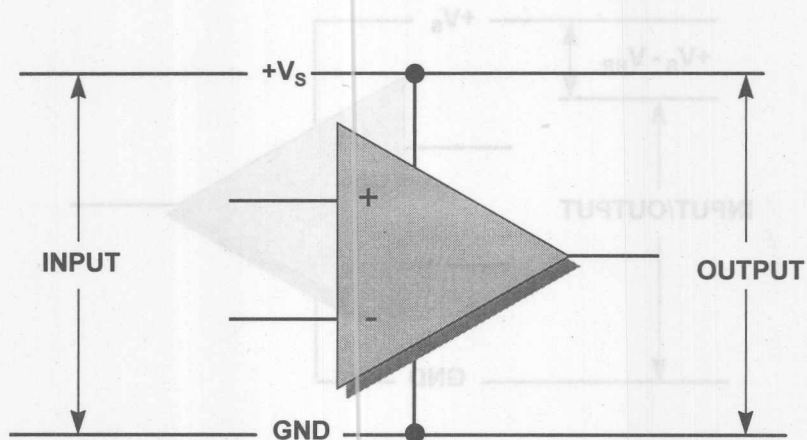
True "Single Supply" Op Amp

- True Single Supply Op Amps Can Operate Down to Their Negative Rail (Ground)
- Sometimes Still Require 2-3 Volts of Headroom V_{HR} Between the Positive Excursion and the Positive Rail.

1 - 21



What is a Rail-Rail Amplifier ? (con't)



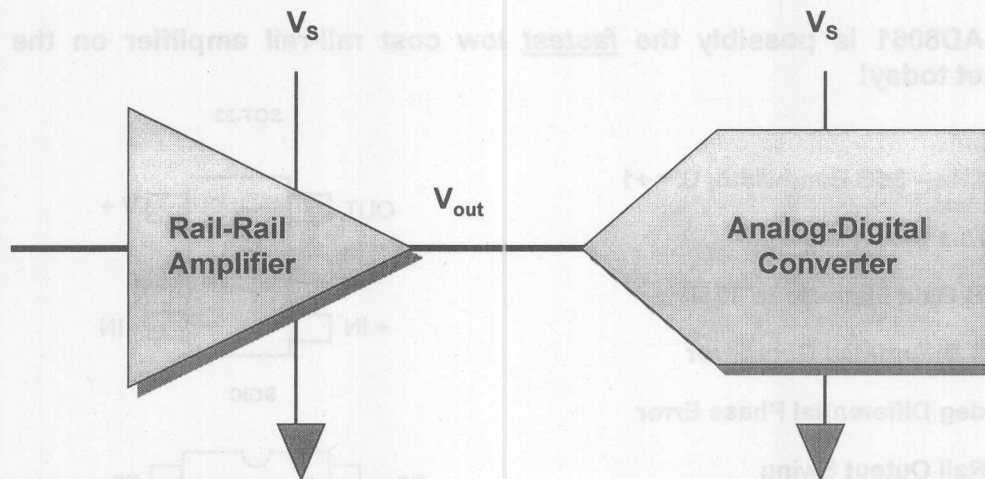
True Rail-Rail Op Amp

- True Rail-Rail Op Amps Can Swing to Within a Few Millivolts of Their Supply Rails, Either on the Input, the Output or Both.

1 - 22



Why Rail-Rail?



- Many New High Speed A-D Converters Operate From Single +3V to +5V Supply
- Rail-Rail Amplifiers Provide Maximum Dynamic Range

1 - 23

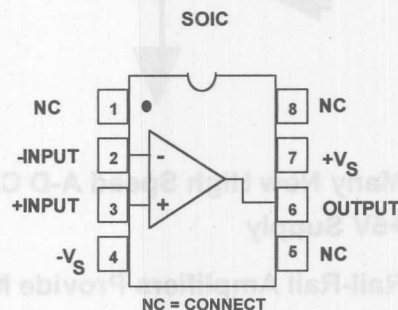
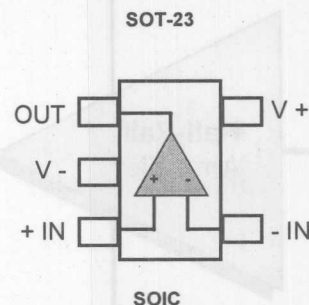


*preliminary

AD8061* 275 MHz, Rail-Rail Amplifier

The AD8061 is possibly the fastest low cost rail-rail amplifier on the market today!

- 275 MHz, - 3dB Bandwidth, $G = +1$
- 900 V/us Slew Rate
- 0.1 dB Gain Flatness to 30 MHz
- 0.01% Differential Gain Error
- 0.05 deg Differential Phase Error
- Rail-Rail Output Swing
- 2.7V to 12V Supplies
- 7.2 mA Typ Supply Current
- - 40 deg C to +85 deg C Operation



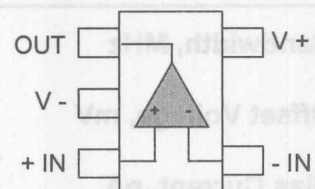
1 - 24



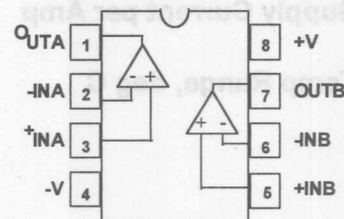
AD8519 and AD8529 8 MHz Single/Dual Rail to Rail Amplifiers

- 8 MHz Unity Gain Bandwidth
- 2.7V/ μ s Slew Rate
- Low Offset Voltage : 1.2 mV max
- Input Voltage Noise : 7 nV/Hz @ 1 kHz
- Rail-Rail Output Swing
- Single Supply Operation : + 2.7V to + 12V
- 8 Pin SOIC and Space Saving SOT-23 Package!
- - 40 deg C to + 125 deg C Operating Range

SOT-23



8 LEAD SOIC
AND
MicroSOIC



1 - 25



CMOS Rail-Rail Amplifiers...A Quick Look

	OP250/450	AD8541/42/44	AD8591/92/94
Bandwidth, MHz	1.0	1.0	3.0
Offset Voltage, mV	2.0	1.0	2.0
Bias Current, pA	2.0	4.0	5.0
Output Current, mA	100	15	250
Supply Current per Amp	800 μ A	45 μ A	700 μ A
Temp Range, deg C	-40/+125	-40/+125	-40/+85

1-28



AD8591, AD8592 and AD8594 3 MHz, CMOS Rail-Rail Amplifiers with Shutdown

- 3 MHz Unity Gain Bandwidth
- 5V/ μ s Slew Rate
- 50 pA Input Bias Current
- High Output Current : 250 mA
- Rail-Rail Input and Output
- Single Supply Operation : 2.7V to 6V
 - Normal Mode : 700 μ A/amplifier
 - SHUTDOWN Mode < 1 μ A
- - 40 deg C to + 85 deg C Operation
- AD8591 : 6 Lead SOT-23
- AD8592 : 10 Lead μ SOIC
- AD8594 :
 - 16 Lead Narrow Body SOIC
 - 16 Lead TSSOP

1 - 27



AD8541, AD8542 and AD8544

Low Power, Low I_B Rail-Rail CMOS Amplifiers

Package Styles:

- 1 MHz Unity Gain Bandwidth
 - 0.8V/ μ s Slew Rate
 - 4 pA Typ Input Bias Current
 - 15 mA Output Current
 - Rail-Rail Input and Output
 - Single Supply Operation : 2.7V to 5.5V
 - Supply Current : 45 μ A/amplifier
 - - 40 deg C to + 125 deg C Operation
- AD8541 : 5 Lead SOT-23, 8 Pin SOIC
 - AD8542 : 8 Lead SOIC, 8 Lead TSSOP
 - AD8544 : 14 Narrow Body SOIC and TSSOP



AD8551*, AD8552* and AD8554* "Zero Drift" Chopper Amplifiers

* Preliminary

The AD8551/52/54 are low cost, single, dual and quad amplifiers that require no external components to achieve virtually "zero drift" performance.

Precision, Low Power Amplifiers

- Virtual "Drift Free" Performance Over Wide C
- Low Input Offset
- Low Input Bias
- Rail-to-Rail Input and Output
- 120 dB PSRR, CMRR
- Overload Recovery < 2 ms
- Single Supply Operation: 2.7V to 5V
- Only 650 nA per amplifier
- 8Pin DIP and SOIC Packages
- -40 deg C to +125 deg Operating Range



**preliminary*

AD8551*, AD8552* and AD8554* “Zero Drift” Chopper Amplifiers

The AD8551/52/54 are low cost, single, dual and quad amplifiers that require no external components to achieve virtually “zero drift” performance!

- Virtual “Drift Free” Performance : 0.03 $\mu\text{V}/\text{deg C}$
- Low Input Offset Voltage : 5 μV
- Low Input Bias Current : 20 pA
- Rail-Rail Input and Output
- 120 dB PSRR, CMRR
- Overload Recovery < 2 ms
- Single Supply Operation : 2.7V to 5V
- Only 650 μA per amplifier
- 8/14 Pin DIP and SOIC Packages
- - 40 deg C to + 125 deg Operating Range

1 - 30



AD8561 and AD8564 6 ns Single and Quad High Speed Comparators

The AD8561 and AD8564 are improved performance, pin-pin upgrades to the LT1010 and MAX901, respectively.

High Speed Comparators

- 6 ns Typical Propagation Delay
- Separate Analog and Digital Supply Pins (AD8564)
- Compatible with TTL/CMOS Logic
- No Active Pull Up Required
- LATCH Function (AD8561)
- 8/16 Pin DIP, SOIC and TSOP Packages
- -40 deg C to +85 deg C Operation



AD8561 and AD8564

6 ns Single and Quad High Speed Comparators

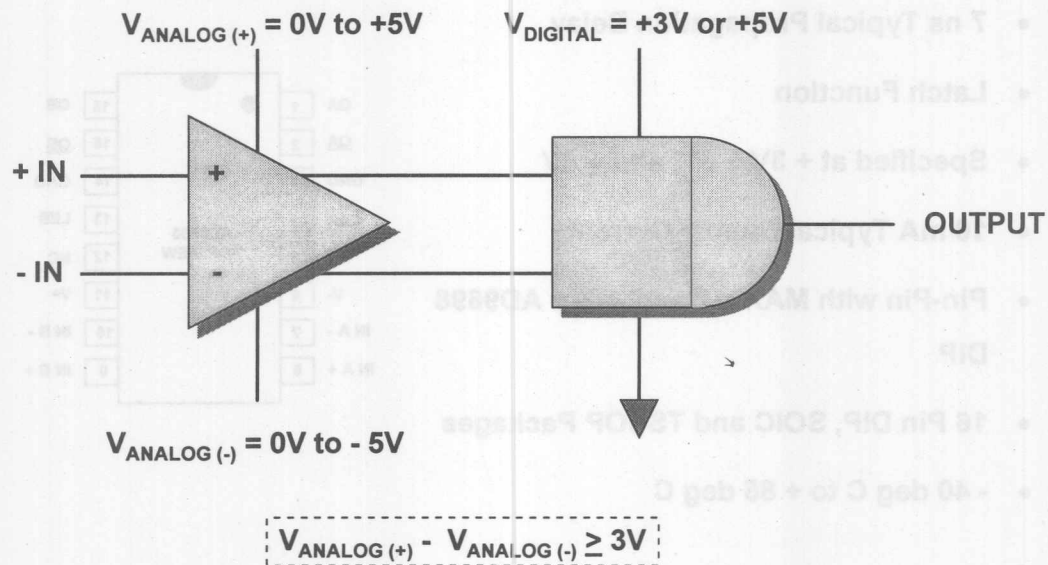
The AD8561 and AD8564 are improved performance, pin-pin upgrades to the LT1016 and MAX901, respectively.

- 6 ns Typical Propagation Delay
- Input Common Mode Range Includes Ground
- Separate Analog and Digital Supply Pins (AD8564)
- Compatible with TTL/CMOS Logic
- No Active Pull Up Required
- LATCH Function (AD8561)
- 8/16 Pin DIP, SOIC and TSSOP Packages
- -40 deg C to + 85 deg C Operation

1 - 32



AD8564 - Block Diagram

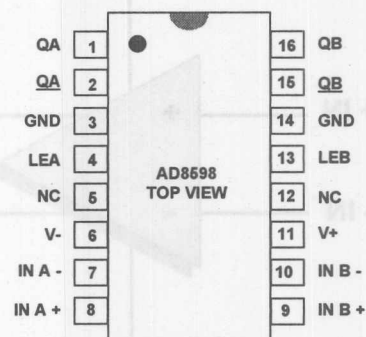


1 - 33



AD8598 Dual High Speed Comparator

- 7 ns Typical Propagation Delay
- Latch Function
- Specified at + 3V + 5V, and $\pm 5V$
- 10 mA Typical Supply Current
- Pin-Pin with MAX912 and ADI's AD9698
DIP
- 16 Pin DIP, SOIC and TSSOP Packages
- - 40 deg C to + 85 deg C





Comparison Between the AD8561/AD8598 and AD9696/AD9698...

The AD8561 (single) and AD8598 (dual) are recommended, pin-pin replacements for the AD9696 and AD9698, respectively, however there are performance differences...

	AD8561	AD9696	AD8598	AD9698
Prop Delay, typ	6.0 ns	4.5 ns	7 ns	4.5 ns
Rise/Fall Times	3.8/1.5 ns	1.9/1.4 ns	3.8/1.5 ns	1.9/1.4 ns
$E_{OS, \max}$	3.0 mV	2.0 mV	7.0 mV	2.0 mV
I_B, \max	5 μ A	55 μ A	6 μ A	55 μ A
$I_{SY, \max}$	6 mA	32 mA	12 mA	64 mA

1 - 35



Comparison Between the AD8581/AD8588 and AD8586/AD8588...

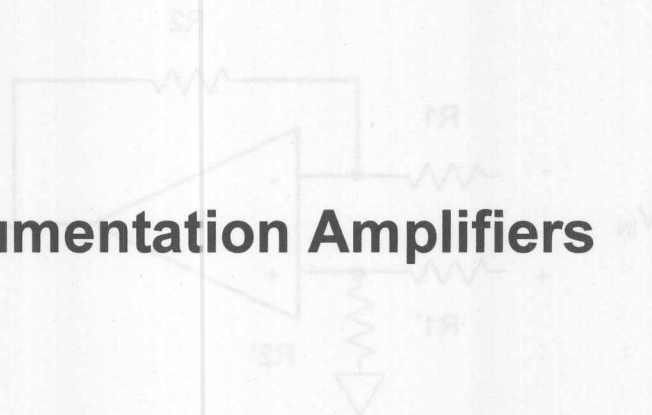
The AD8581 (single) and AD8588 (dual) are recommended pin-pin replacements for the AD8586 and AD8588, respectively, however there are performance differences...

AD8581	AD8586	AD8588	AD8588
Prop Delay, typ	6.0 ns	4.5 ns	4.5 ns
Rise/Fall Times	3.8/3.8 ns	3.8/3.8 ns	3.8/3.8 ns
$E_{OL, max}$	3.0 mV	2.0 mV	2.0 mV
$I_{OL, max}$	5 μ A	8 μ A	8 μ A
$I_{AV, max}$	8 mA	32 mA	32 mA

1-38



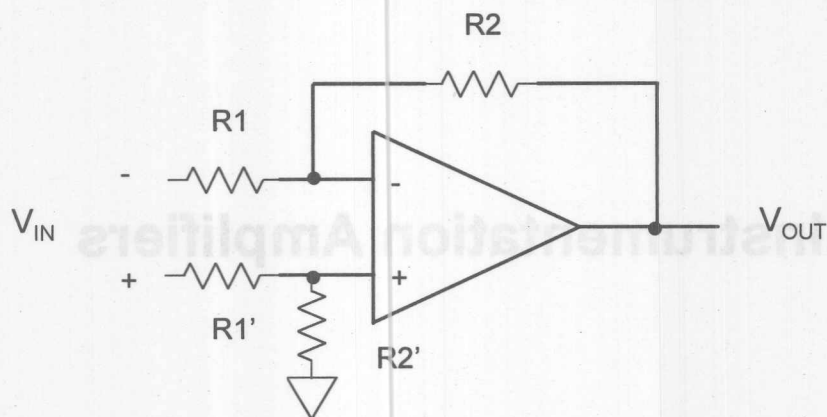
Instrumentation Amplifiers



- For Balanced Gain, $G = R2/R1 = R3/R1$
- For Balanced input E , $R1 = R2 = R3$
- Common Mode Rejection Depends on Resistor Ratio Matching



A "Differential" Amplifier

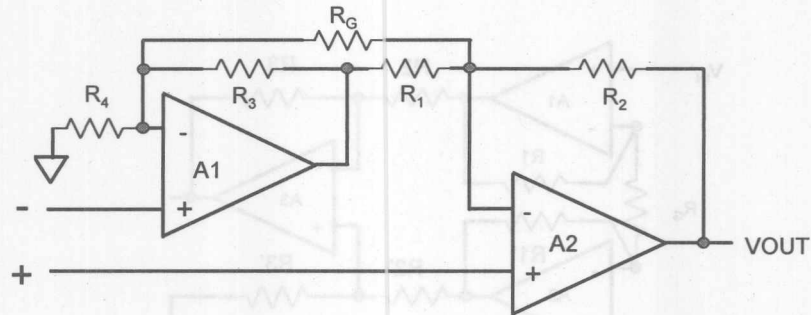


- For Balanced Gain, $G = R2/R1 = R2'/R1'$
- For Balanced Input Z, $R1' + R2' = R1$
- Common Mode Rejection Depends on Resistor Ratio Matching

1 - 38



2 Op Amp Design



$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_G}$$

- **Advantages:**

- Requires Only 2 Op Amps
- High Input Impedance

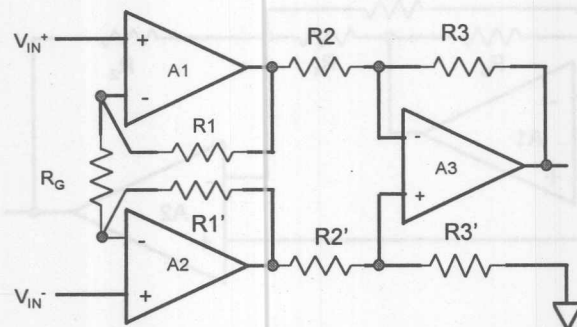
- **Disadvantages:**

- Input Common Mode Voltage Range Is Gain-Dependent
- A1 Amplifies Common Mode by $(R_3+R_4)/R_4$

1 - 38



3 Op Amp Design



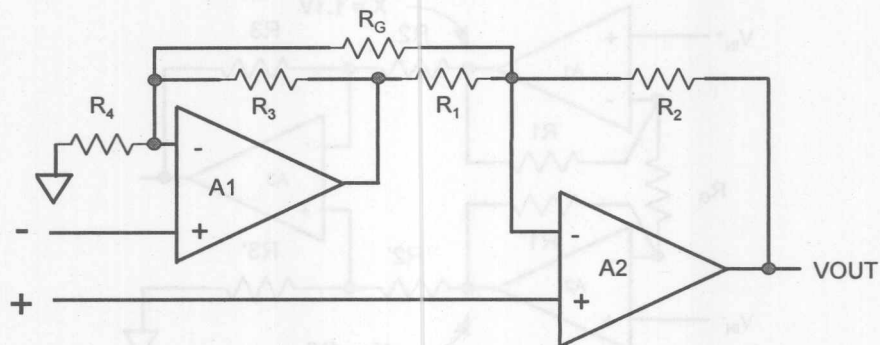
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{2R1}{R_G} + 1 \right) \left(\frac{R3}{R2} \right)$$

- **Advantages:**
 - Fully Differential Inputs
 - Very High Input Impedance
 - Input Common Mode Voltage Range Is No Longer Gain-Dependent
- **Disadvantage : Extra Amplifier**

1 - 40



A Discrete Instrumentation Amp using Rail-Rail Op Amps...

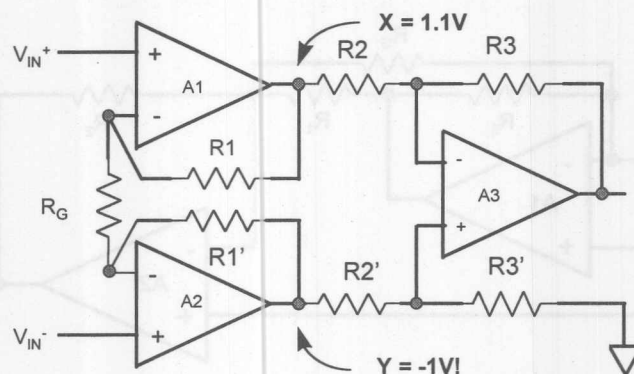


- A 2 Op-Amp in-Amp Will Operate on a Single Supply but.....
- A1 Amplifies the Common Mode Voltage. At Low in-Amp Gain, A1 Operates at High Gain. This Limits Input Voltage Range
- A1 and A2 Operate at Different Gains and Therefore Have Different Closed Loop Bandwidths. This Reduces CMRR at Higher Frequencies

1 - 41



A Discrete Instrumentation Amp using Rail-Rail Op Amps...



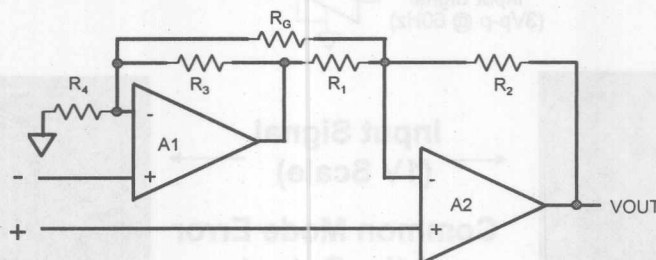
- In an in-Amp Using 3 Precision Single Supply, R/R Op-Amps + Matched R'S, the Input Common-Mode Voltage Range Will Not Be Able to Go to Ground.
- As the Common-Mode Voltage Decreases, Internal Node (Y) Will Attempt to Go Below Ground and Will Clamp at the Negative Rail!!!

1 - 42



AD627 Micropower, Rail-Rail Instrumentation Amplifier

...With Rail-to-Rail Outputs!

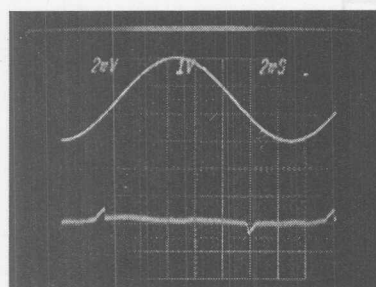
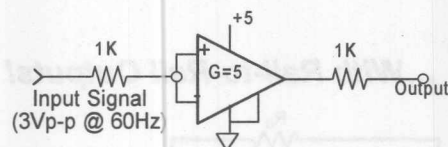


- Gain Range : 5-1,000
- 0.05% Max Gain Error
- 10 ppm/deg C Max Gain Drift
- 75 μ V Max Input Offset Voltage
- 10 nA Max Input Bias Current
- 80 kHz Bandwidth
- 50 nV/Hz RTI Noise @ 1 kHz
- -50mV to + 3.5V CMV Range
- 85 dB CMRR (G=5)
- +3V to \pm 15V Supply Options
- 50 μ A Supply Current
- 8 Pin DIP, SOIC Packages

1-43



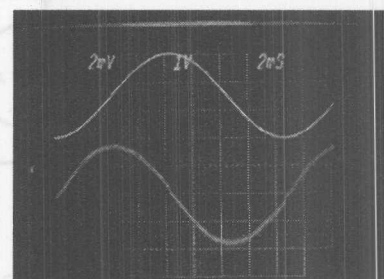
AD627 Competitive Advantage



AD627
G=5

Input Signal
(1V Scale)

Common Mode Error
at the Output
(2mV Scale)



INA 122
G=5

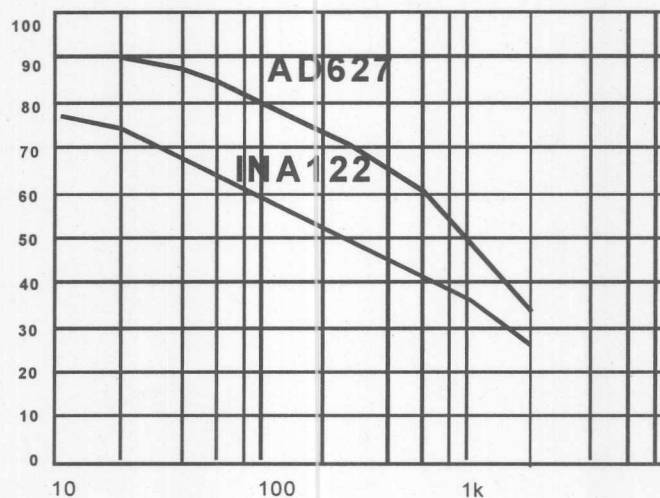
AD627 common mode error = $500\mu\text{V}$
INA 122 common mode error = 7mV

The INA 122 gives you 10x the error!



AD627 Competitive Advantage

The AD627 Has Superior Common Mode Rejection Performance Over Frequency!



AD627 vs. INA122 CMRR vs. Frequency

1 - 45



AD627 Competitive Advantage

The AD627 Has Superior Common Mode Rejection Performance Over Frequency



AD627 vs. INA122 CMRR vs. Frequency

1-46



SECTION 2

ANALOG SIGNAL PROCESSING

Log Amplifiers and Detectors

Modulators and Mixers

Digitally Controlled, Variable Gain Line Drivers

2-1



SECTION 2 ANALOG SIGNAL PROCESSING

Digitally Controlled, Variable Gain Line Drivers
Modulators and Mixers
Log Amplifiers and Detectors

2-2

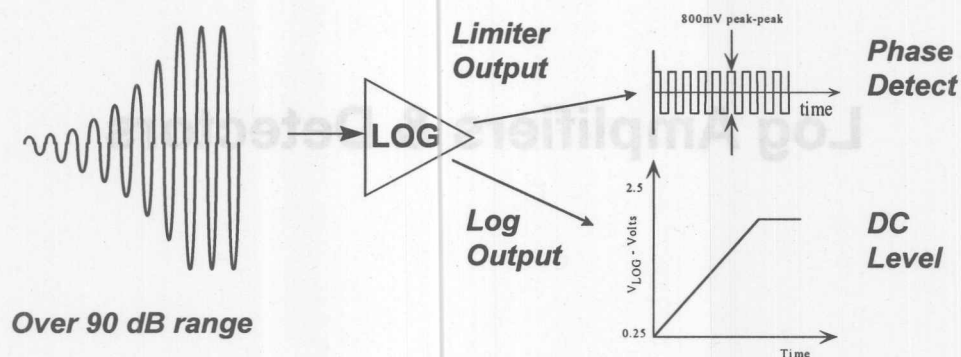


Log Amplifiers & Detectors



Where Are Log Amps Used?

Measuring Widely Varying RF/IF Signals (Wide Dynamic Range)...



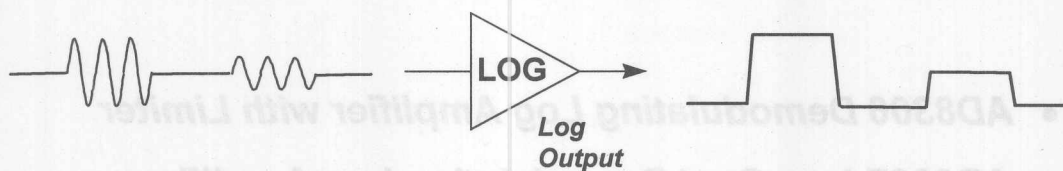
Limiter Output useful for Quadrature Phase Shift Keying (QPSK) , Frequency Shift Keying (FSK), or Amplitude Shift Keying (ASK - Edge Detection)

2-4



Where Are Log Amps Used?

Detecting Low Level/Varying Signal Envelopes (RF Burst or Pulse Detection)...



Detect RF signals from μV to V & linear-in-dB



Analog Devices Introduces 4 New Low Cost, High Speed Log Amplifiers...

- **AD8306 Demodulating Log Amplifier with Limiter**
- **AD8307 Low Cost Demodulating Log Amplifier**
- **AD8309 Low Cost Demodulating Log Amplifier
w/Limiter**
- **AD8313 Power Detector/Controller**

2-6



ADI's New Log Amp Family...

	AD8306	AD8307	AD8309	AD8313
Frequency	350 MHz	500 MHz	350 MHz	2500 MHz
Dynamic Range	95 dB	92 dB	95 dB	65 dB
Limiter Output	Yes	No	Yes	No
Log Accuracy	± 0.4 dB	± 1.0 dB	± 1.0 dB	± 1.0 dB
Power Supply	3V to 5V	3V to 5V	3V to 5V	3V to 5V
Package	TSSOP-16	SO-8	TSSOP-16	Micro SO-8

2-7



*** Preliminary**

AD8306*

350 MHz, 95 dB Demodulating Log Amp with Limiter

- Usable to 350 MHz
- -80 dBm to +15 dBm Dynamic Range
- ± 0.4 dB Log Linearity
- -80 dBm Limiter Sensitivity
- ± 50 ps Limiter Phase Skew
- 1 nV/ $\sqrt{\text{Hz}}$ Spectral Noise Density
- 69 mW Typical Power Consumption
- User programmable Intercept & Slope
- +3V & +5V Single Supply Operation

2-8



AD8309 Low Cost, Demodulating Log Amp with Limiter

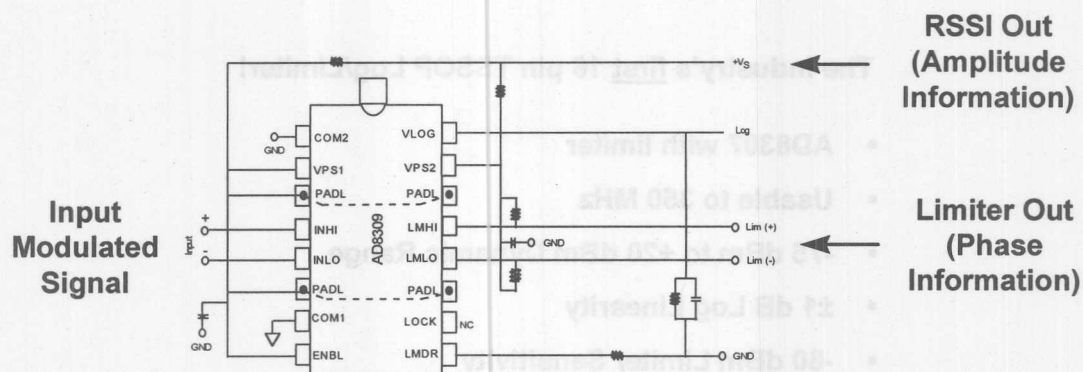
The Industry's first 16 pin TSSOP Log/Limiter!

- AD8307 with limiter
- Usable to 350 MHz
- -75 dBm to +20 dBm Dynamic Range
- ± 1 dB Log Linearity
- -80 dBm Limiter Sensitivity
- ± 100 ps Limiter Phase Skew
- $1 \text{ nV}/\sqrt{\text{Hz}}$ Spectral Noise Density
- 72 mW Typical Power Consumption
- User programmable Intercept & Slope
- +3V & +5V Single Supply Operation

2-9



AD8309 - Simplified Diagram



The hard limiter removes the amplitude variation from the input signal giving a square wave out which varies with phase.

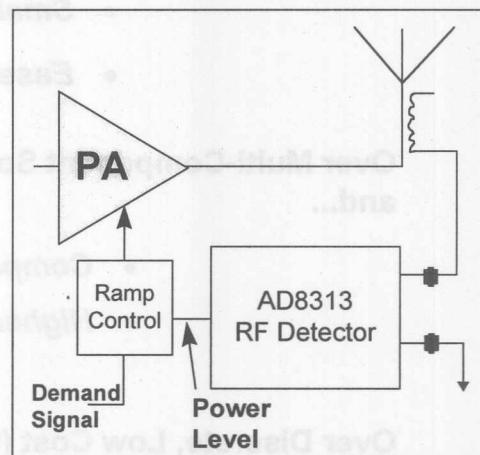
Note that the AD8309 has 4 paddle pins which are tied high. These are down-bonded to the paddle to help eliminate package parasitics.

2-10



AD8313 0.1 to 2.5GHz, Power Detector/Controller

- Designed to Directly Measure Tx RF Power. No Mix-Down Required.
- Output Is Log Proportional to Tx Power
- 0.1 To 2.5 GHz Input Signal
- 100 ns Response Time
- 65 dB Dynamic Range
- +/-1dB Accuracy (50 dB Range)
- +2.7V to +5V Operation, $I_{sy} = 15mA$
- 8 Pin Micro-SOIC Package



2-11



The AD8313 Offers the RF Designer the Advantages of ...

- *Lower Total Cost*
- *Smaller Packaging*
- *Ease of Design*

Over Multi-Component Solutions (Log Amps, Mixers, etc),
and...

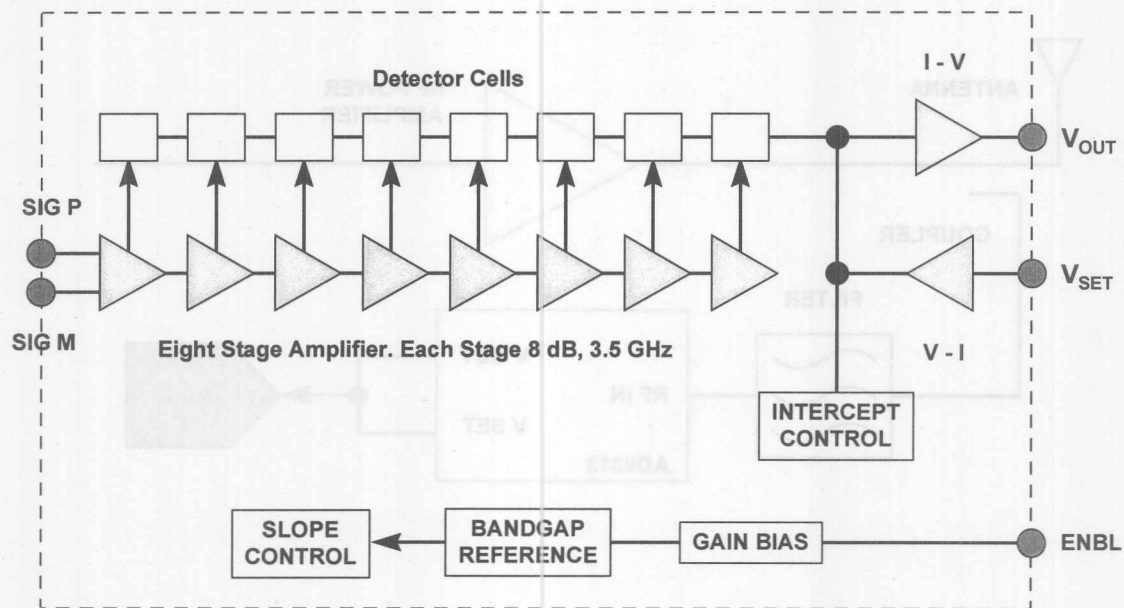
- *Comparable Cost*
- *Higher Performance*

Over Discrete, Low Cost (\$3-4) Diodes Which are Very Non-
Linear and Highly Temperature Dependent

2-12



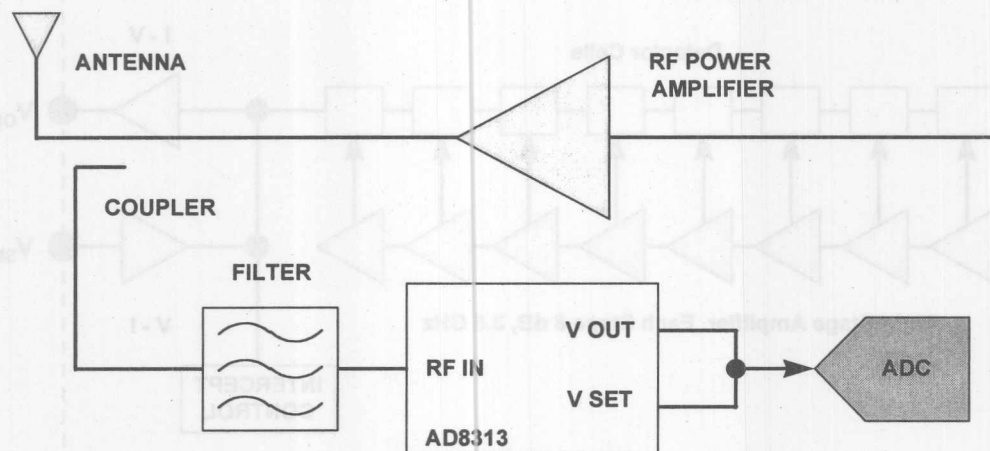
AD8313 Simplified Block Diagram



2-13



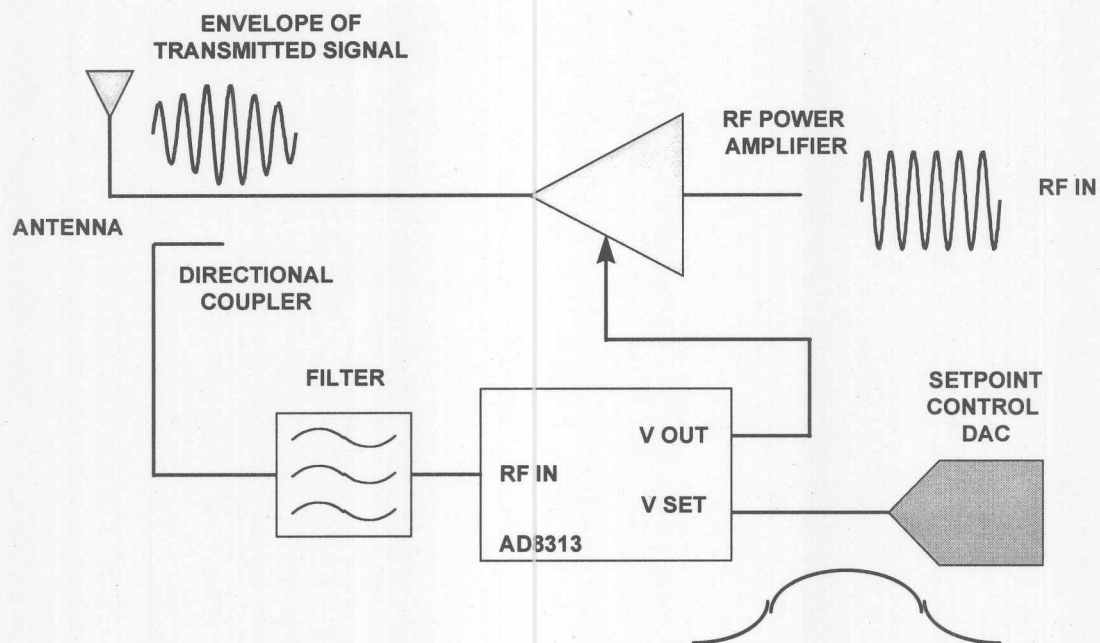
AD8313 Typical Application : Measurement Mode



2-14



AD8313 Typical Application : "Set Point Controller Mode"



2-15



2-16



Modulators and Mixers

- 10 Pin Mini-SO and 14 Pin TSOP Packages
- Single Supply Operation : 5V @ 40 mA
- 50 ohm RF Port Input Z
- Differential LO, RF and IF Ports
- P1 dB : +10 dBm
- Low Noise Figure : 12 dB
- Low LO Drive : -10 dBm
- Two-Port As Either an Up or Down Converter
- Doubly-Balanced "Gilbert Cell" Mixer

The AD8343 is a low distortion, wide dynamic range monolithic mixer optimized for transmit but equally suited for receive applications

800 - 2500 MHz High IP3 Mixer
AD8343*

* Preliminary



*** Preliminary**

AD8343* **800 - 2500 MHz High IP3# Mixer**

The AD8343 is a low distortion, wide dynamic range monolithic mixer optimized for transmit but equally suited for receive applications

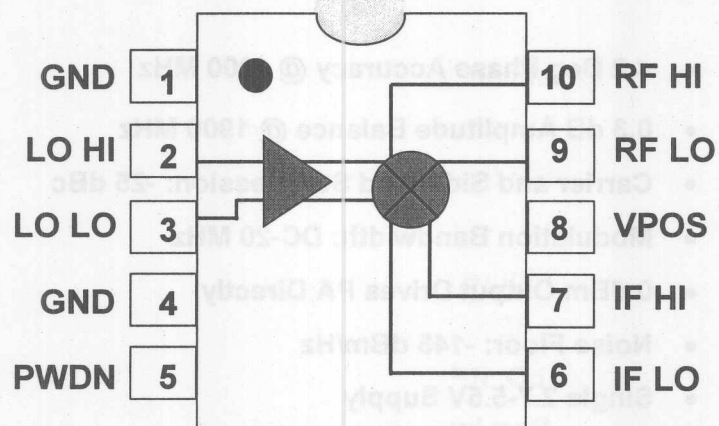
- Doubly-Balanced "Gilbert Cell" Mixer
- Usable As Either an Up or Down Converter
- Two Tone IP3# Input : + 20 dBm @ 1800 MHz
- Low LO Drive : - 10 dBm
- Low Noise Figure : 12 dB
- P1 dB : + 10 dBm
- Differential LO, RF and IF Ports
- 50 ohm RF Port Input Z
- Single Supply Operation : 5V @ 40 mA
- 10 Pin Mini-SO and 14 Pin TSSOP Packages

= 3rd Order Intercept

2-18



AD8343 Functional Block Diagram



2-19



*** Preliminary**

AD8346* **800-2500 MHz Direct I and Q Modulator**

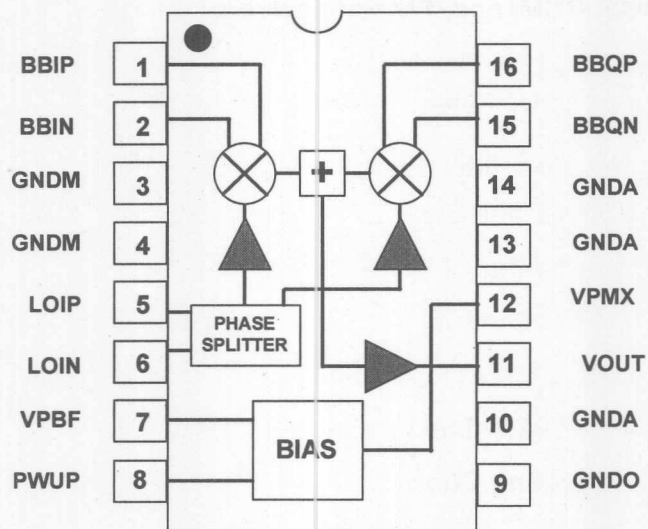
The AD8346 can be used as the transmit modulator in digital systems such as PCS, DCS, GSM, and ISM transceivers.

- **< 2 Deg Phase Accuracy @ 1900 MHz**
- **0.3 dB Amplitude Balance @ 1900 MHz**
- **Carrier and Sideband Suppression: -25 dBc**
- **Modulation Bandwidth: DC-20 MHz**
- **0 dBm Output Drives PA Directly**
- **Noise Floor: -145 dBm/Hz**
- **Single 2.7-5.5V Supply**
- **Operating Current: 60mA**
- **Standby Mode: 20 μ A**
- **Compact 16-pin SSOP Package**

2 - 20



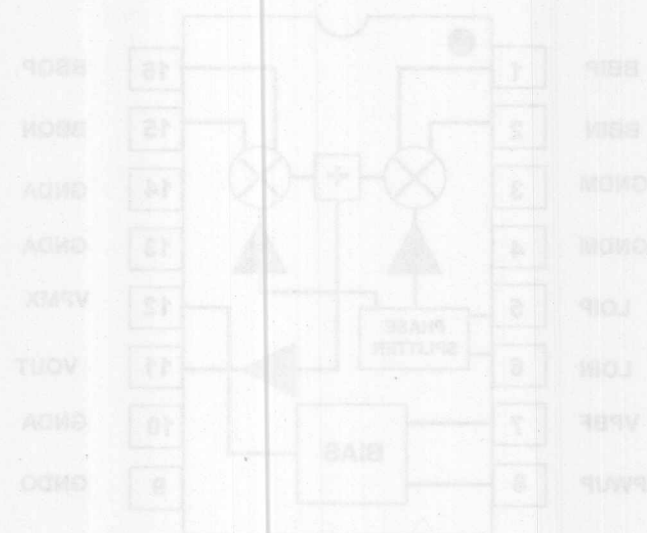
AD8346 Functional Block Diagram



2-21



AD8346 Functional Block Diagram



2 - 22



AD8320, AD8321 Digitally Controlled, Variable Gain Line Drivers

The AD8320 and AD8321 are the industry's first MCNS-DQCS[®] compliant line drivers to feature a variable gain range that supports all cable modems.



Multimedia Cable Network System - Data Over Cable Interface Standard

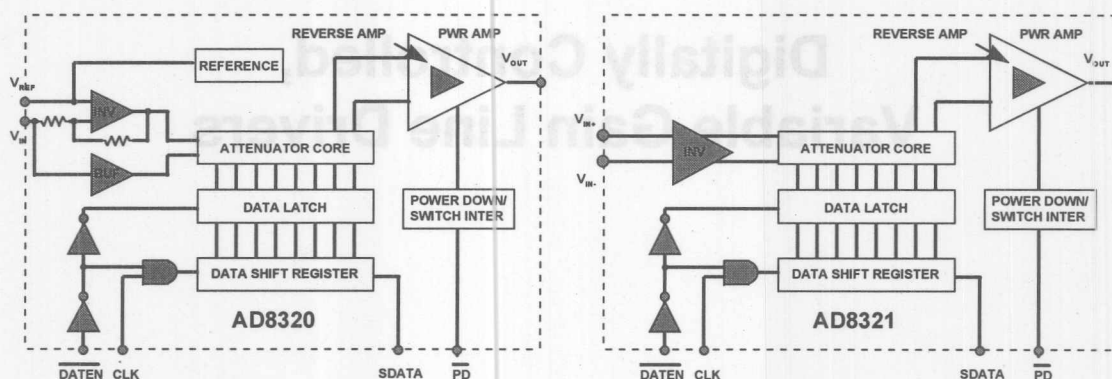
2-23



*** Preliminary**

AD8320, AD8321* Digitally Controlled, Variable Gain Line Drivers

The AD8320 and AD8321 are the Industry's first MCNS-DOCIS* compliant line drivers to feature a variable gain range that supports all cable modems



*Multimedia Cable Network System - Data Over Cable Interface Standard

2 - 24

**AD8320, AD8321 Key Model Differences**

	AD8320	AD8321
<i>Serial Input</i>	8 bit	7 bit
<i>Gain Range</i>	36 dB	53 dB
<i>Scale Factor</i>	V/V/LSB	dB/LSB
<i>Output Level</i>	12 dBm	18 dBm
<i>Bandwidth</i>	DC - 150 MHz	DC - 235 MHz
<i>Power Supply</i>	5V to 12V	5V to 10V

The AD8320 and AD8321 are pin compatible!

2 - 25



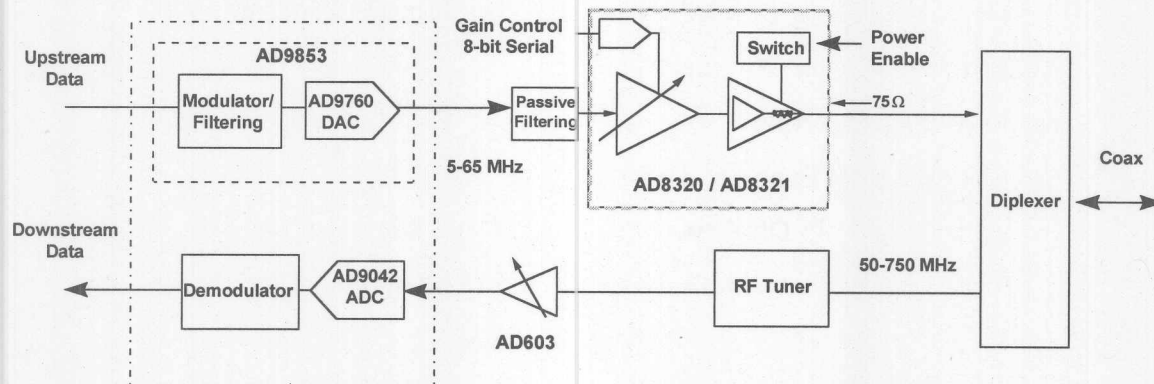
AD8320, AD8321 : Key Specs and Features

- **Drives Low Distortion Signals into 75 ohms :**
 - **-57 dBc SFDR @ 42 MHz and 12 dBm Output**
 - **-46 dBc SFDR @ 42 MHz and 18 dBm Output (AD8320, only)**
- **No Line Transformer Required**
- **Single Supply Operation**
- **Power Down (PD) Feature:**
 - **Logic “0” Shuts Off Power Amplifier (Disables Output)**
 - **Turns on Reverse Amplifier to Maintain 75 ohms @ $V_{cc}/2$ at Output Port**
- **SPI[™]-Compatible Serial Interface**
- **20 Pin Thermally Enhanced Power SOIC Package**
- **- 40 deg C to + 85 deg C Operation**

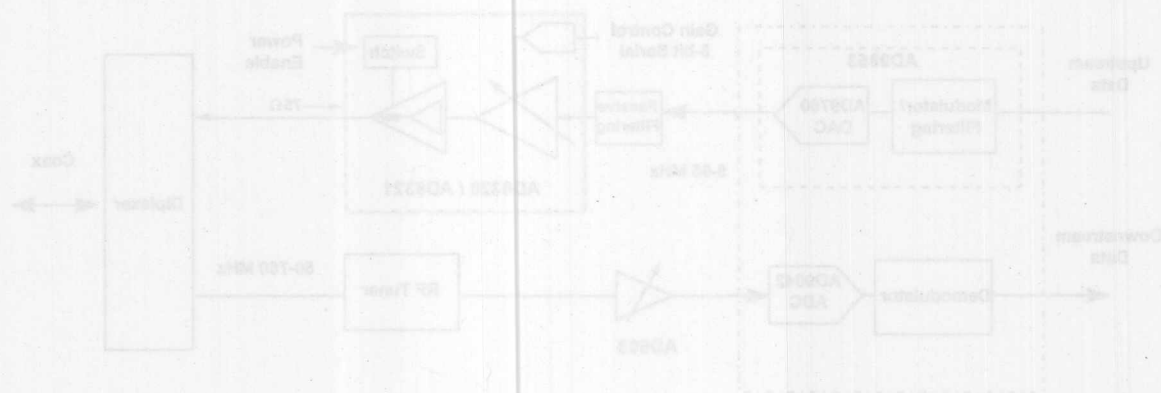
2 - 26



THE AD9853 & AD8320 in an Application for up-Stream Transmit in Subscriber-End Cable Modems



2 - 27



2-28



SECTION 3

ANALOG-DIGITAL CONVERTERS

High Speed

Single Supply, Low Power

High Resolution

Voltage - Frequency - Voltage

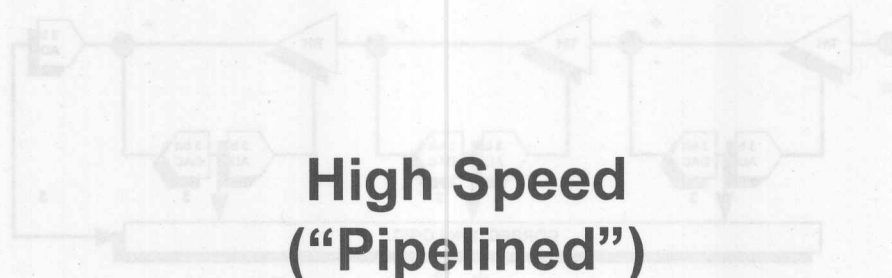
Sigma Delta



SECTION 3 ANALOG-DIGITAL CONVERTERS

High Speed
Single Supply, Low Power
High Resolution
Voltage - Frequency - Voltage
Sigma Delta

3-2

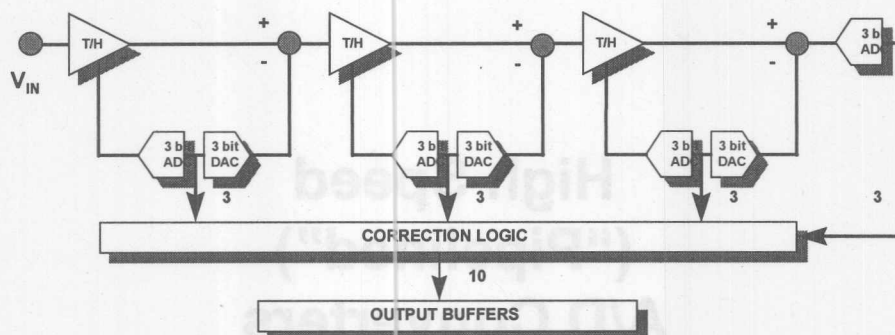


High Speed ("Pipelined") A/D Converters

A pipelined ADC generates its result by performing a series of low resolution conversions (3 bit in this case) beginning with the MSB. All results generated are subtracted from the original signal (using reconstruction DACs) before the next element in the pipeline (another 3-bit ADC) performs a conversion on the remainder. The correction logic corrects the data, aligns it correctly, uses the extra bits (2 in this case) to perform error correction and outputs a 10-bit result.



“Pipelined” or Multi-Stage Architecture...



A pipelined ADC generates its result by performing a series of low resolution conversions (3 bit in this case) beginning with the MSBs.

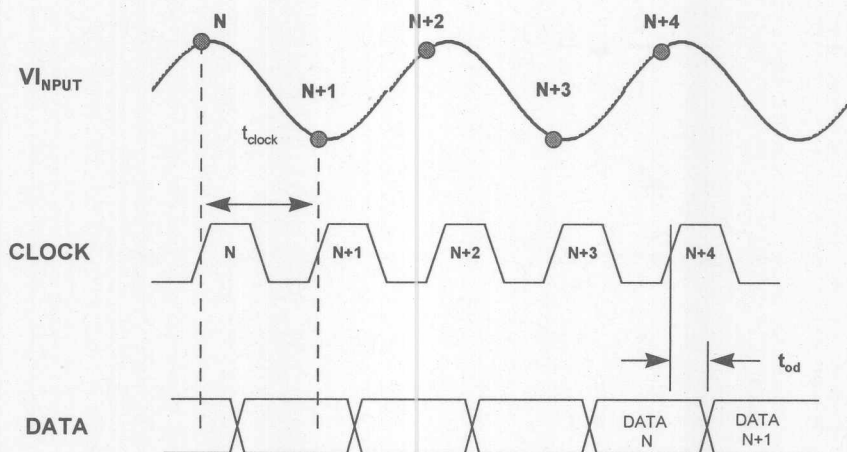
All results generated are subtracted from the original signal (using reconstruction DACs) before the next element in the pipeline (another 3-bit ADC) performs a conversion on the remainder.

The correction logic collects the data, aligns it correctly, uses the extra bits (2 in this case) to perform error correction and outputs a 10-bit result.

3 - 4



Timing Diagram for a Typical Pipelined A/D Converter

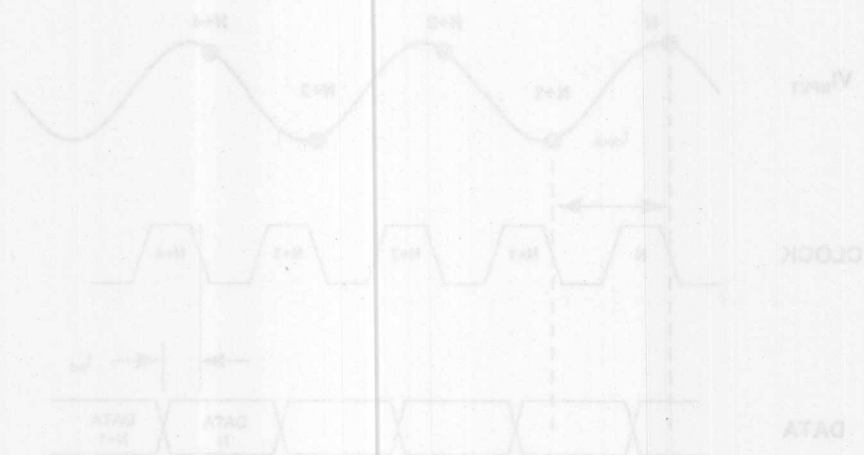


The ADC converts at a high speed ($>1\text{MHz}$) but there is a latency of 4 clock cycles from the start of a conversion to the appearance of the result at the output. The output data rate is, however equal to the clock rate

3-5



Timing Diagram for a Typical Pipelined A/D Converter

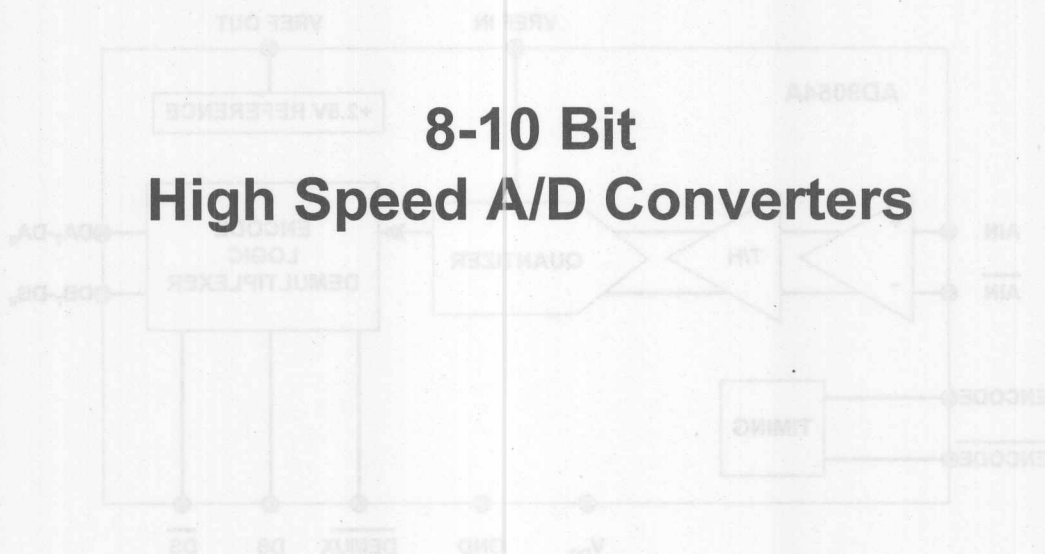


The ADC converts at a high speed (>1MSPS) but there is a latency of 4 clock cycles from the start of a conversion to the appearance of the result at the output. The output data rate is, however, equal to the clock rate.

3-6



8-10 Bit High Speed A/D Converters

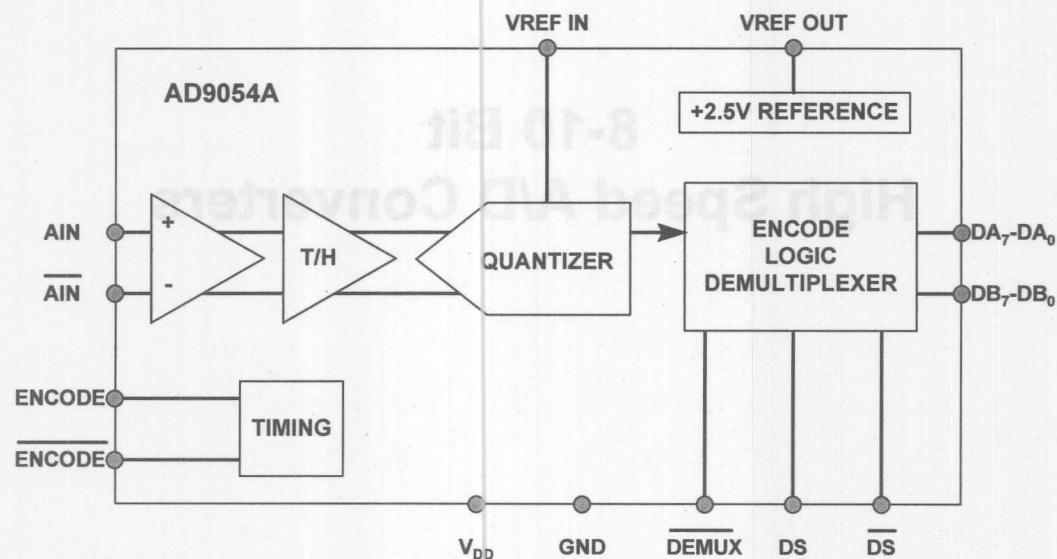




Preliminary
Information

AD9054A* 8 Bit, 135/200 MSPS A/D Converter

The AD9054A is design-optimized for digitizing analog RGB graphics signals for LCD monitors and/or video scan converters.



3-8



AD9054A Key Specs and Features

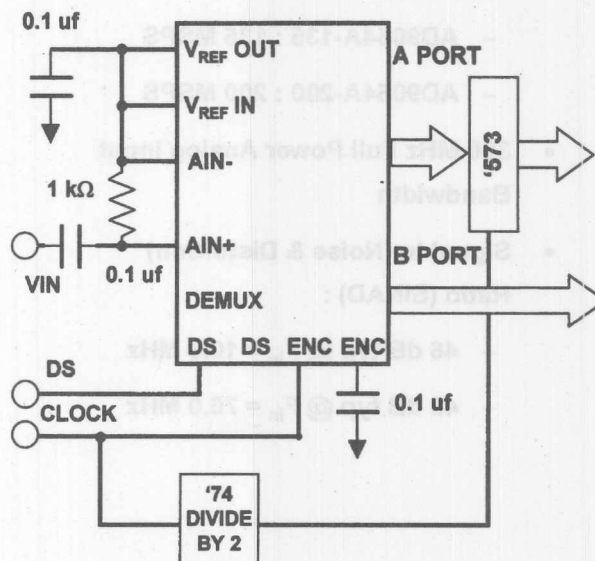
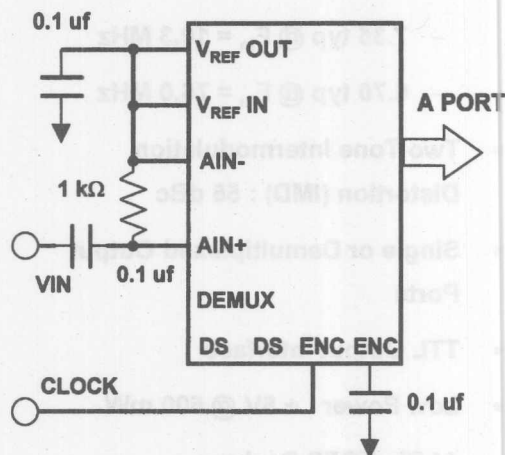
($F_{\text{encode}} = 200 \text{ MHz}$ unless otherwise specified)

- Two Speed Versions :
 - AD9054A-135 : 135 MSPS
 - AD9054A-200 : 200 MSPS
- 380 MHz Full Power Analog Input Bandwidth
- Signal to (Noise & Distortion) Ratio (SINAD) :
 - 46 dB typ @ $F_{\text{in}} = 10.3 \text{ MHz}$
 - 42 dB typ @ $F_{\text{in}} = 76.0 \text{ MHz}$
- Effective Number of Bits (ENOB) :
 - 7.35 typ @ $F_{\text{in}} = 10.3 \text{ MHz}$
 - 6.70 typ @ $F_{\text{in}} = 76.0 \text{ MHz}$
- Two Tone Intermodulation Distortion (IMD) : 55 dBc
- Single or Demultiplexed Output Ports
- TTL Output Interface
- Low Power : + 5V @ 500 mW
- 44 Pin TQFP Package

3-9



AD9054A : Single vs Dual Port Mode

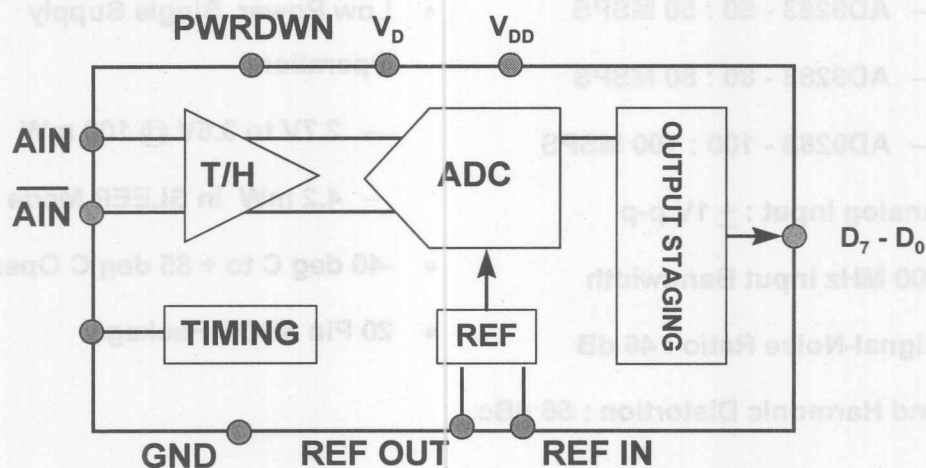


3-10



AD9283 8 Bit, 100 MSPS A/D Converter

The AD9283 has been optimized for low cost, low power, small size and ease of programming. Applications include battery-powered instruments, hand held scopemeters or low cost digital oscilloscopes



3-11



AD9283 - Key Specs and Features

($F_{in} = 41 \text{ MHz}$)

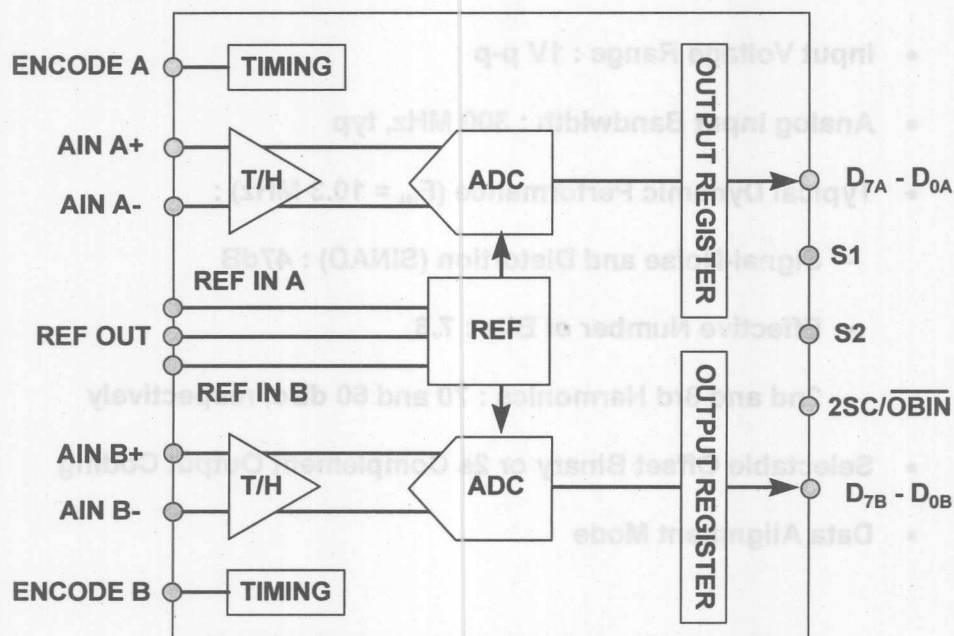
- **Three Speed Versions :**
 - AD9283 - 50 : 50 MSPS
 - AD9283 - 80 : 80 MSPS
 - AD9283 - 100 : 100 MSPS
- **Analog Input : $\pm 1\text{V}$ p-p**
- **300 MHz Input Bandwidth**
- **Signal-Noise Ratio : 46 dB**
- **2nd Harmonic Distortion : 56 dBc**
- **Effective Number of Bits : 7.0**
- **Low Power, Single Supply Operation:**
 - 2.7V to 3.6V @ 100 mW
 - 4.2 mW in SLEEP Mode
- **-40 deg C to + 85 deg C Operation**
- **20 Pin SSOP Package**

3-12



* Preliminary
Information

AD9288* **Dual 8 Bit, 40/80/100 MSPS A/D Converter**



3-13



AD9288 - Key Specs and Features

- Input Voltage Range : 1V p-p
- Analog Input Bandwidth : 300 MHz, typ
- Typical Dynamic Performance ($F_{IN} = 10.3$ MHz) :
 - Signal-Noise and Distortion (SINAD) : 47dB
 - Effective Number of Bits : 7.6
 - 2nd and 3rd Harmonics : 70 and 60 dBc, respectively
- Selectable Offset Binary or 2s Complement Output Coding
- Data Alignment Mode

3 - 14



AD9288 - Key Specs and Features (con't)

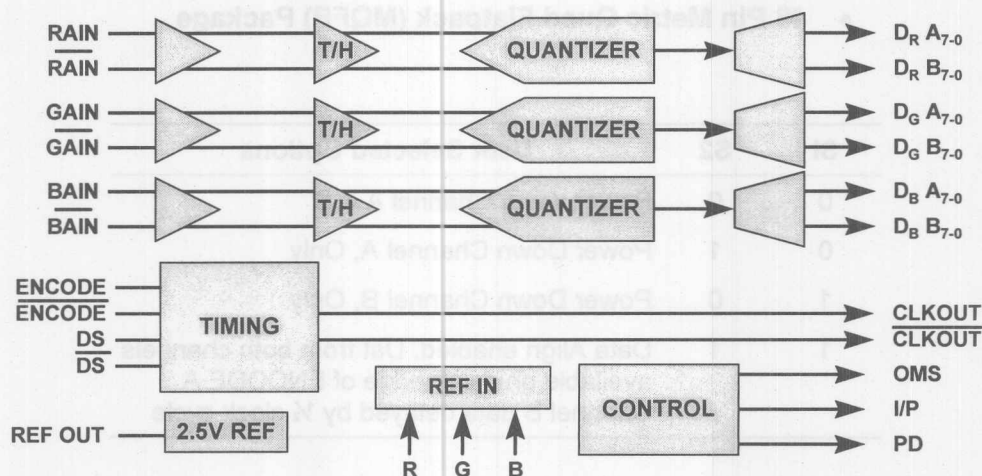
- Single +3V Operation :
 - 90 mW Power Dissipation per Channel
 - Power Down Mode : 6 mW per Channel
- 48 Pin Metric Quad Flatpack (MQFP) Package

SI	S2	User Selected Options
0	0	Power down Channel A & B
0	1	Power Down Channel A, Only
1	0	Power Down Channel B, Only
1	1	Data Align enabled. Dat from both channels available on rising edge of ENCODE A. Channel B data delayed by ½ clock cycle



AD9483 Triple 8 Bit, 135 MSPS A/D Converter

The AD9483 is design-optimized for digitizing RGB (Red-Green-Blue) graphics signals from personal computers and workstations with displays up to 1280 x 1024 @ 75 Hz.



3-16



AD9483 - Key Specs and Features

(F_{IN} = 49.7 MHz)

- 300 MHz Analog Input Bandwidth
- Signal to (Noise & Distortion) Ratio (SINAD) : 43 dB
- Effective Number of Bits (ENOB) : 6.8 typ
- Two Tone Intermodulation Distortion (IMD) : 55 dBc
- TTL, CMOS or PECL-Compatible ENCODE Input
- 3.3V/5.0V Three State CMOS Digital Outputs
- Single or Dual Channel (Demultiplexed) Output Ports
- Single Supply Operation :5V
- 100 Pin MFQP (Metric Quad Flat Pack)
- 0 deg C to +85 deg C Operation

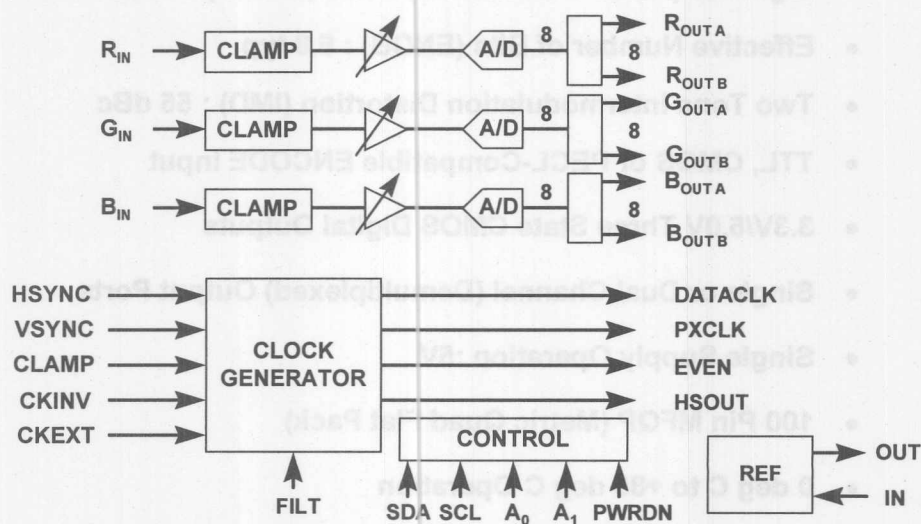
3 - 17



* Preliminary

AD9884* Triple 8 Bit, 140 MSPS Graphics Digitizer

The AD9884 is a complete monolithic graphics digitizer optimized for digitizing RGB graphics signals from personal computers and workstations





AD9884 - Key Specs and Features

- **300 MHz Full Power Bandwidth Supports 1280 x 1024 Resolution @ 75 Hz**
- **On-Board PLL Generates Pixel Clock from 20-140 MHz**
- **PLL Clock Jitter Typically Only 500 ps peak-peak**
- **0.5 - 1.0 Volt Input Range**
- **Internal 1.25V Reference**
- **Programmable Gain and CLAMP Control**
- **Low Power : 3.3V @ 800 mW, typ**
- **128 Lead MQFP Package**
- **0 deg C to + 85 deg C Operation**

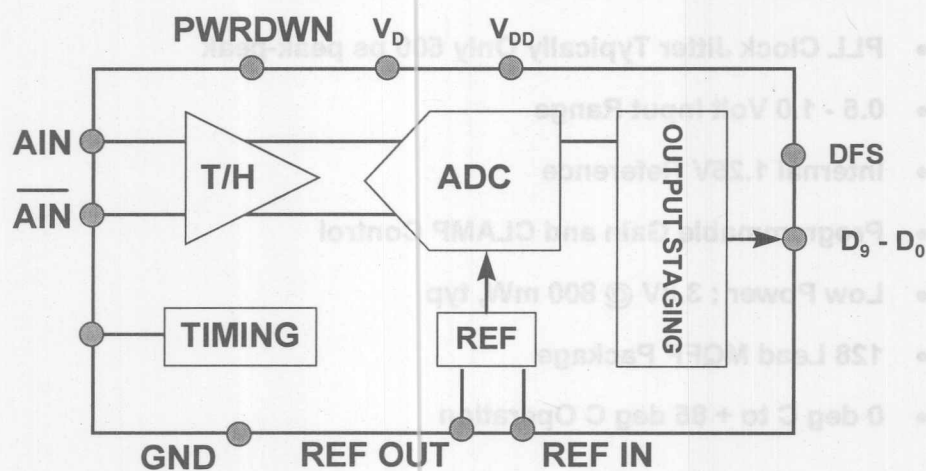
3 - 19



* Preliminary

AD9214* 10 Bit, 65/80/100 MSPS A/D Converter

The AD9214 has been optimized for low cost, low power, small size and ease of programming. Applications include battery-powered instruments, hand held scopemeters or low cost digital oscilloscopes



3 - 20



AD9214 : Key Specs and Features

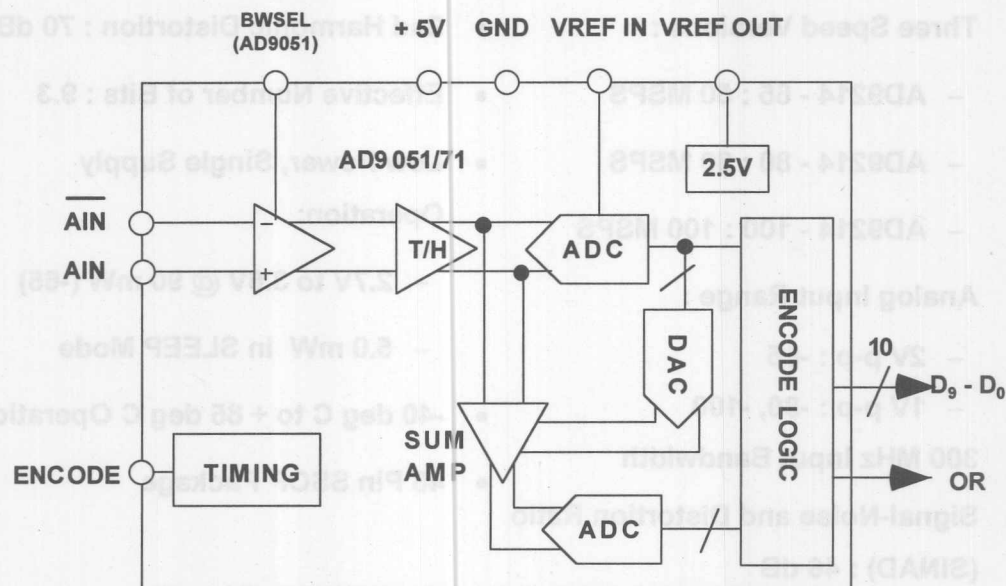
($F_{IN} = 10.3 \text{ MHz}$)

- Three Speed Versions :
 - AD9214 - 65 : 50 MSPS
 - AD9214 - 80 : 80 MSPS
 - AD9214 - 100 : 100 MSPS
- Analog Input Range :
 - 2V p-p : -65
 - 1V p-p : -80, -100
- 300 MHz Input Bandwidth
- Signal-Noise and Distortion Ratio (SINAD) : 46 dB
- 2nd Harmonic Distortion : 70 dBc
- Effective Number of Bits : 9.3
- Low Power, Single Supply Operation:
 - 2.7V to 3.6V @ 90 mW (-65)
 - 5.0 mW in SLEEP Mode
- -40 deg C to + 85 deg C Operation
- 48 Pin SSOP Package

3 - 21



AD9071 and AD9051 10 Bit, 60/100 MSPS Sampling A/D Converters



3 - 22

**AD9071 and AD9051 Key Specs and Features**

	AD9071	AD9051
<i>Sampling Rate</i>	100 MSPS	60 MSPS
<i>Analog Bandwidth</i>	280 MHz	50/130 MHz
<i>SINAD¹</i>	56 dB	57 dB
<i>ENOB¹</i>	9.2 bits	9.3 bits
<i>2nd Harmonic¹</i>	- 75 dB	-73 dBc
<i>Two Tone IMD¹</i>	- 70 dBc	-65 dBc
<i>Package Style</i>	28 pin SOIC	28 pin SSOP
<i>Power Dissipation</i>	450 mW	250 mW

1) $f_{in} = 10.3 \text{ MHz}$

3 - 23



AD9071 and AD9051 : Add'l Specs and Features

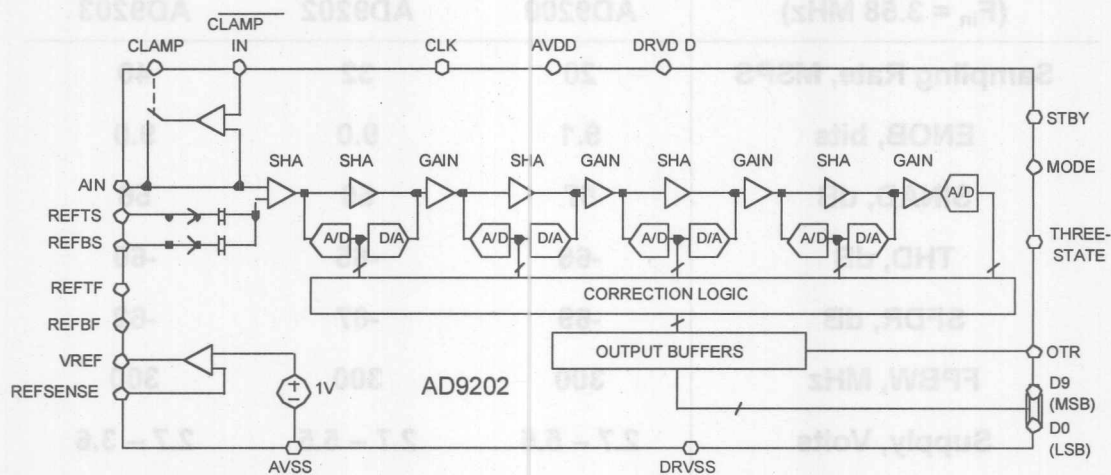
- TTL-Compatible Input Logic
- +5V/+3.3V CMOS-Compatible Output Logic
- Analog Input Voltage Range :
 - AD9051 : 1.25 V p-p
 - AD9071 : 1.00 V p-p
- Single Supply Operation : + 5V
- Out-of-Range Indicator
- -40 deg C/+85 deg C Operation



*** Preliminary
Information**

AD9202 and AD9203* 10 Bit, 32/40 MSPS A/D Converters

The AD9202 and AD9203 are pin-compatible, next generation upgrades to our popular AD9200



3-25



Performance Comparison between the AD9200 and the AD9202/AD9203...

($F_{in} = 3.58 \text{ MHz}$)	AD9200	AD9202	AD9203
Sampling Rate, MSPS	20	32	40
ENOB, bits	9.1	9.0	9.0
SINAD, dB	57	56	56
THD, dB	-66	-65	-60
SFDR, dB	-69	-67	-62
FPBW, MHz	300	300	300
Supply, Volts	2.7 – 5.5	2.7 – 5.5	2.7 – 3.6
Power, mW	80	95	50

3 - 26



AD9202, AD9203 - Additional Specs and Features...

- **IF Undersampling to 135 MHz**
- **Adjustable On-Board Reference**
- **Out-Of-Range Indicator**
- **Built-In CLAMP Function for DC Restoration of Video Signals**
- **Three-State Digital Outputs**
- **Power Down Mode : < 5 mW**
- **Package Style :**
 - **AD9202 : 28 Pin SSOP**
 - **AD9203 : 28 Pin SSOP and TSSOP**
- **-40 to 85 deg C Operating Temperature Range**

3 - 27



AD9202, AD9203 - Additional Specs and Features...

- IF Undersampling to 135 MHz
- Adjustable On-Board Reference
- Out-Of-Range Indicator
- Built-in CLAMP Function for DC Restoration of Video Signals
- Three-State Digital Outputs
- Power Down Mode : < 5 mW
- Package Style :
 - AD9202 : 28 Pin SSOP
 - AD9203 : 38 Pin SSOP and TSOP
- -40 to 85 deg C Operating Temperature Range

3 - 28



Preliminary
Information

AD9224, AD9225 and AD9226* 12 Bit, High Speed A/D Converters

The AD9224, AD9225 and AD9226 represent ADI's next generation of high speed, single supply, 12 bit CMOS A/D's, that feature an impressive 12 bit performance.

AD9224 AD9225 AD9226

Throughput Rate (MSPS)	25	50
FP Input	200	80
Signal to (Noise & Distortion) (dB) ¹	68.5	65.5
Total Harmonic Distortion (dB) ¹	-61.0	-60.5
Spurious-Free Dynamic Range (dB) ¹	-63.0	-70.5
Power Dissipation, max (mW)	375	475

Note 1: Measured @ $f_s = 10\text{MHz}$

3 - 29

Preliminary
Information

AD9224, AD9225 and AD9226* 12 Bit, High Speed A-D Converters

The AD9224, AD9225 and AD9226 represent ADI's next generation of high speed, single supply, 12 bit CMOS ADC's, that feature an impressive 12 bit performance!

	AD9224	AD9225	AD9226
Throughput Rate (MSPS)	40	25	50
FP Input Bandwidth (MHz)	120	105	200
Signal to (Noise & Distortion) (dB) ¹	65.5	69.6	70
Total Harmonic Distortion (dB) ¹	-68.8	-81.0	-80.0
Spurious-Free Dynamic Range (dB) ¹	-70.8	-83.0	-83.0
Power Dissipation, max (mW)	475	375	600

Note 1 : Measured @ $F_s = 10.0\text{MHz}$

3 - 30

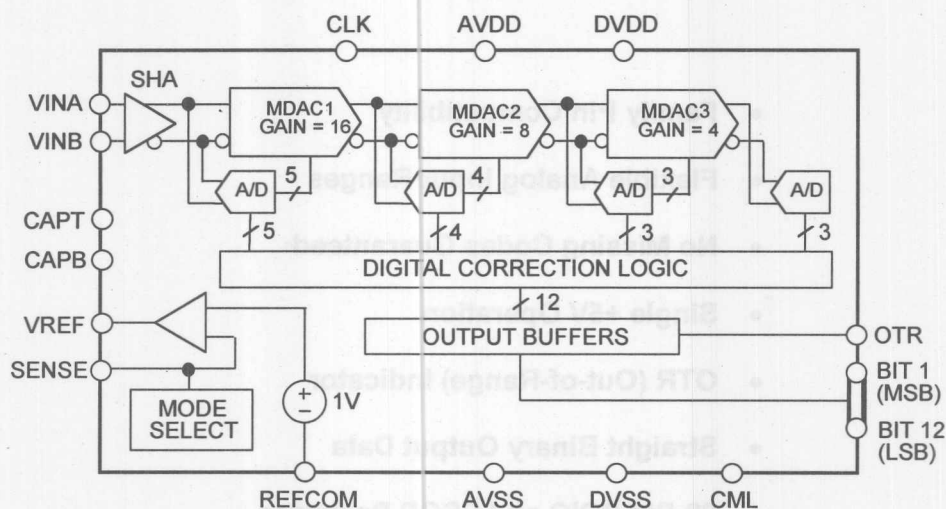


AD9224 - AD9226 : Additional Specs and Features...

- Family Pin Compatibility
- Flexible Analog Input Ranges
- No Missing Codes Guaranteed
- Single +5V Operation
- OTR (Out-of-Range) Indicator
- Straight Binary Output Data
- 28-Pin SOIC and SSOP Packages



AD9224 - AD9226 : Simplified Diagram

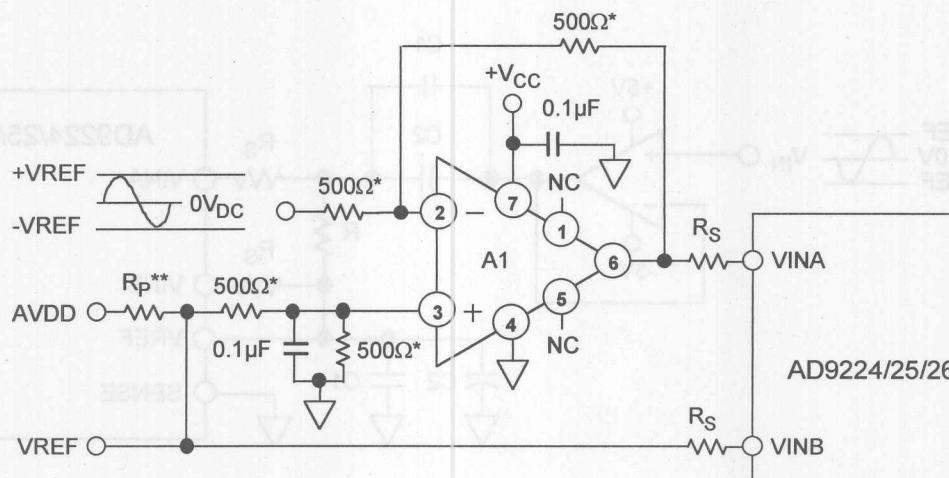


The AD9224-AD9226 employ a unique, multi-stage “pipelined” architecture with digital output error correction logic to achieve 12-bit accuracy at the specified data rates and to guarantee no missing codes over the full operating temperature range

3 - 32



Single-Ended Input with DC Coupled Level Shift



*OPTIONAL RESISTOR NETWORK-OHMTEK ORNA500D

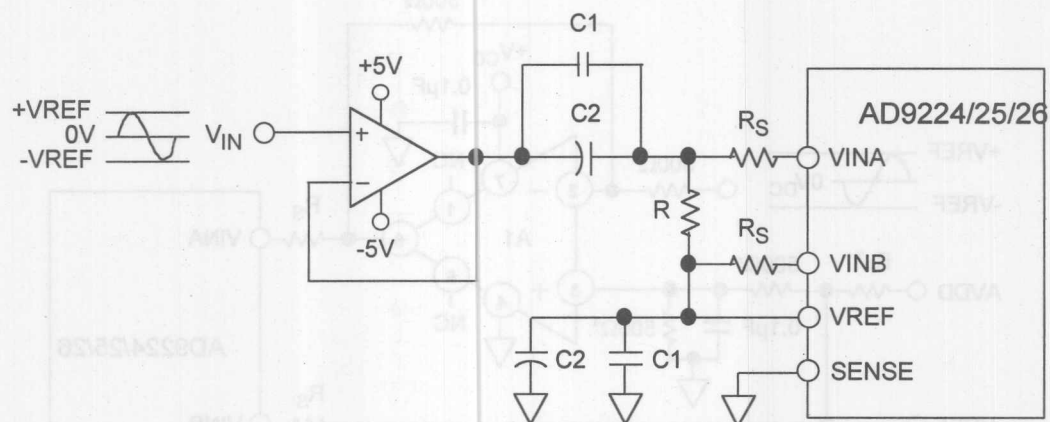
**OPTIONAL PULL-UP RESISTOR WHEN USING INTERNAL REFERENCE

VREF sets the common mode voltage of the AD9224/25/26. Resistors R_s (100 ohms) provide a balanced input impedance to VINA and VINB.

3 - 33



Single-Ended, AC Coupled Input



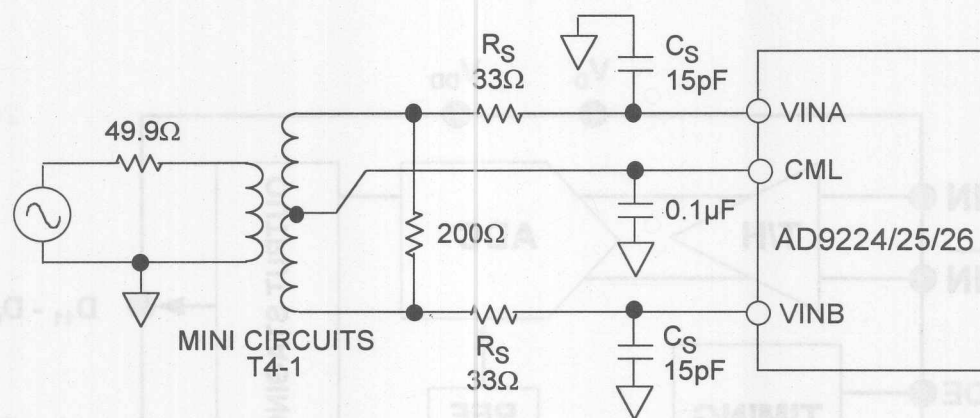
Optimum circuit for noise performance and THD; it provides the ability to use a $+5V$ or $\pm 5V$ op amp.

$$F_{-3dB} = 1/\{2 \times \pi \times R/2 \times (C1 + C2)\}$$

3 - 34



Differential (Transformer-Coupled) Input



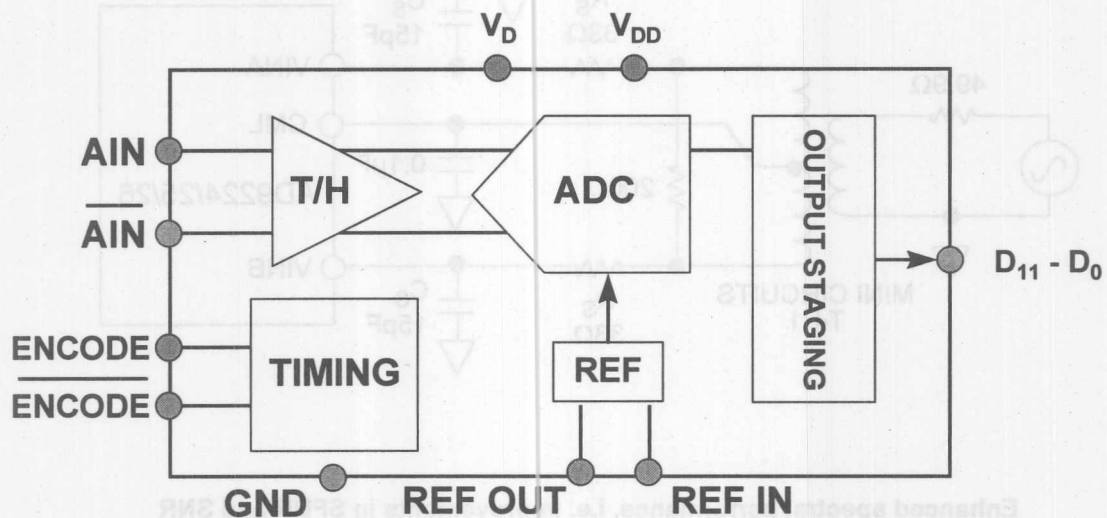
Enhanced spectral performance, i.e. improvements in SFDR and SNR

3 - 35



Preliminary
Information

AD9432* **12 Bit 100 MSPS A/D Converter**



3 - 36



AD9432 - Key Specs and Features

- **Analog Input Range : $\pm 1V$ p-p**
- **Analog Input Bandwidth : 500 MHz**
- **Dynamic Performance ($F_{in} = 47$ MHz) :**
 - **Signal to Noise and Distortion (SINAD) : 65 dB**
 - **Effective Number of Bits : 10.5**
 - **2nd and 3rd Harmonic Distortion : 71 dBc**
- **Two's Complement (2sc) Output**
- **52 Pin Plastic Quad Flatpack (PQFP) Package**
- **5V Power Supply - 750 mW Dissipation**

3 - 37



AD9432 - Key Specs and Features

- Analog Input Range : $\pm 1V$ p-p
- Analog Input Bandwidth : 800 MHz
- Dynamic Performance ($F_{in} = 47$ MHz) :
 - Signal to Noise and Distortion (SNAD) : 66 dB
 - Effective Number of Bits : 10.5
 - 2nd and 3rd Harmonic Distortion : 71 dBc
- Two's Complement (2ac) Output
- 52 Pin Plastic Quad Flatpack (PQFP) Package
- 5V Power Supply - 750 mW Dissipation



CCD/CIS Imaging Processors

- 48 Lead LQFP Package
- + 3V Single Supply Operation, 150 mW
- Two Auxiliary 8 Bit DACs
- Internal Voltage Reference
- Direct ADC Input with Input Clamp
- AUX Input with Input Clamp and PGA

3 - 39



AD9803

10 Bit, 18 MSPS CCD Signal Processor

The AD9803 is a complete CCD and Video Signal Processor developed for electronic cameras

- 3-Wire I/F for Digital Control
- Low Noise PGA with 0-30 dB Range
- Analog Pre-Blanking Function
- AUX Input with Input Clamp and PGA
- Direct ADC Input with Input Clamp
- Internal Voltage Reference
- Two Auxiliary 8 Bit DACs
- + 3V Single Supply Operation, 150 mW
- 48 Lead LQFP Package

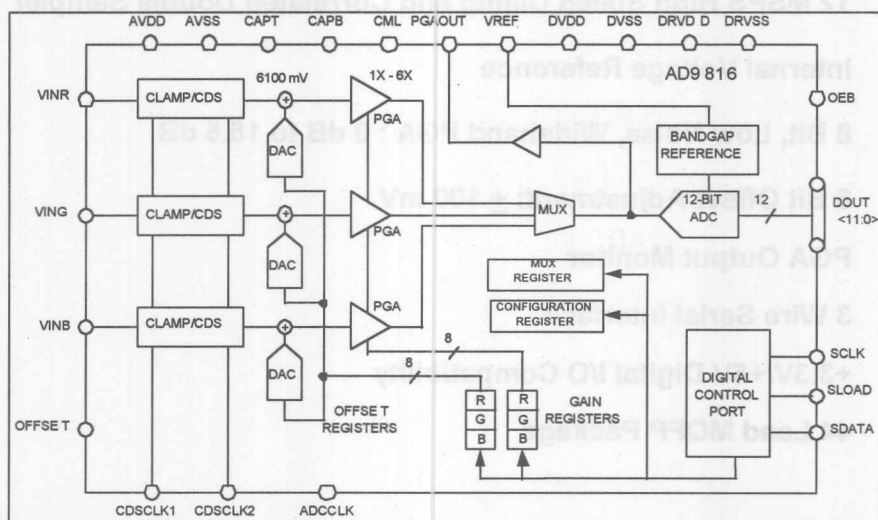
3 - 40



AD9816

12 Bit, 6 MSPS CCD/CIS Signal Processor

The AD9816 is a complete analog signal processor for CCD and CIS applications. Included is all the necessary circuitry to perform 3 channel conditioning and sampling for a variety of imaging applications

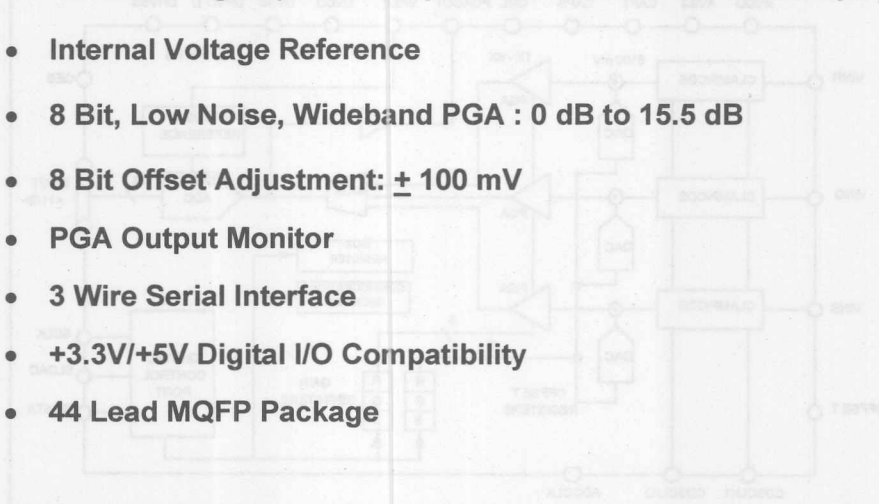


3-41



AD9816 - Key Specs and Features

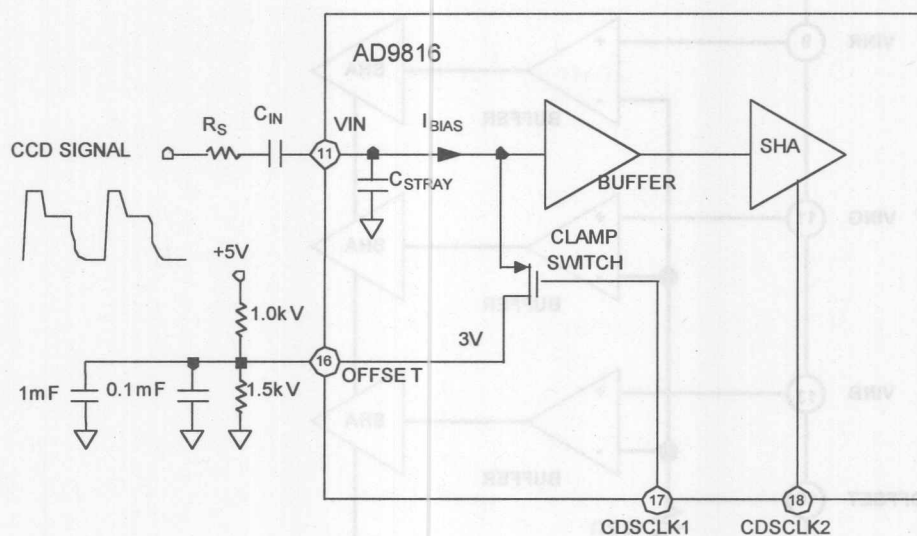
- No Missing Codes Guaranteed
- 3 Channel or 1 Channel Operation
- 12 MSPS High Speed Clamp and Correlated Double Sampler
- Internal Voltage Reference
- 8 Bit, Low Noise, Wideband PGA : 0 dB to 15.5 dB
- 8 Bit Offset Adjustment: ± 100 mV
- PGA Output Monitor
- 3 Wire Serial Interface
- +3.3V/+5V Digital I/O Compatibility
- 44 Lead MQFP Package



3-42



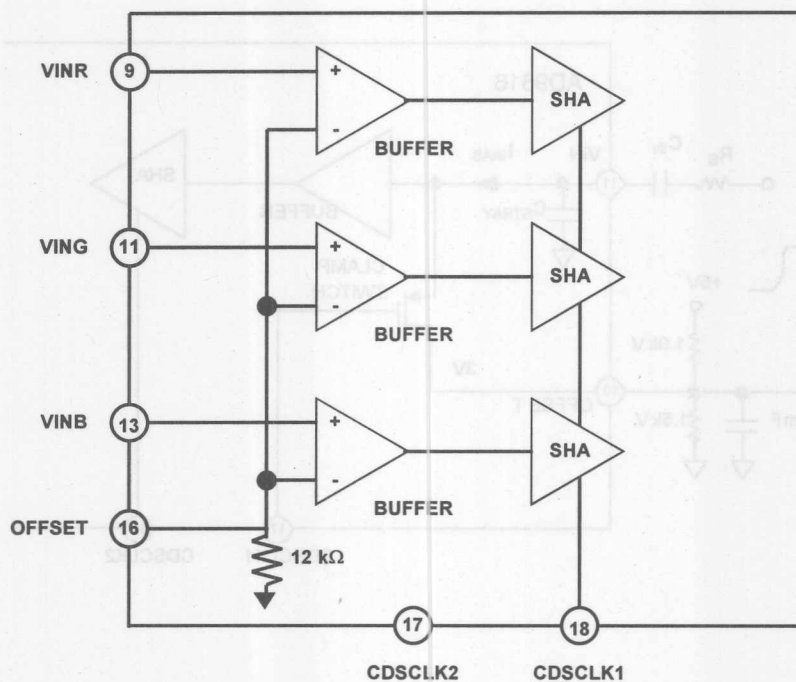
CDS Mode Equivalent Input Circuit



3-43



SHA Mode Equivalent Input Circuit



3-44



Single Supply, Low Power A/D Converters

3 - 45



8-12 Bit A/D Converters

3 - 46



A Preview of ADI's Latest A/D Converter Families...

AD7816-AD7818 :

- Complete A/D : REF, CLK, T/H
- 10 Bit, 100 ksps
- Rail-Rail Inputs
- On-Board Temp Sensor
- Serial Output

AD7416 - AD7418 :

- Same as AD7816-AD7818
- I²C Output

AD7470 - AD7476 :

- 10-12 Bit, 500ksps - 2 MSPS
- Parallel/Serial
- No Int REF or CLK

AD7814 - AD7815 :

- 10 Bit Digital Temp Sensor
- SOT-23 Package
- SPI Interface

AD7492, AD7495 :

- Same as AD747X
- 12 Bit, 1.75 MSPS
- On-Board REF

NEW!



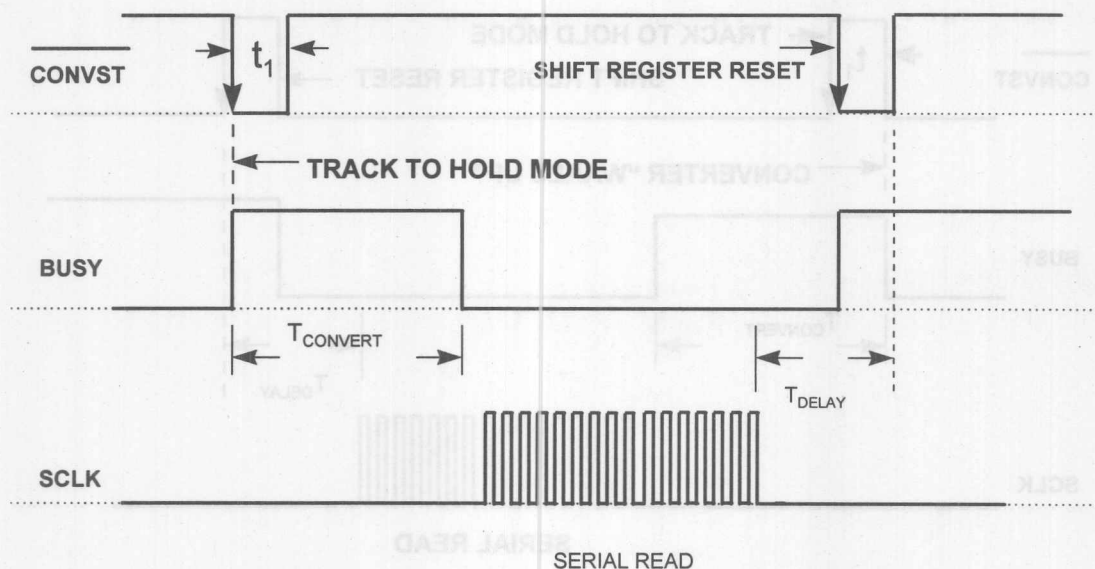
AD781X and AD741X - Key Specs and Features

- Rail to Rail (0 to V_{DD}) Analog Input Range
- 1.2V to V_{DD} Reference Input Range
- On-Board Reference, Track/Hold and Clock
- Operating Supply Range from 2.7V to 5.5V
- Significant Power Savings via, -
 - Reduction in Throughput Rate
 - Power Down (SLEEP) Between Conversions
- -40/-55 deg C to +105/+125 deg C Temp Ranges

3 - 48



How Does the Auto Power Down Feature Work?

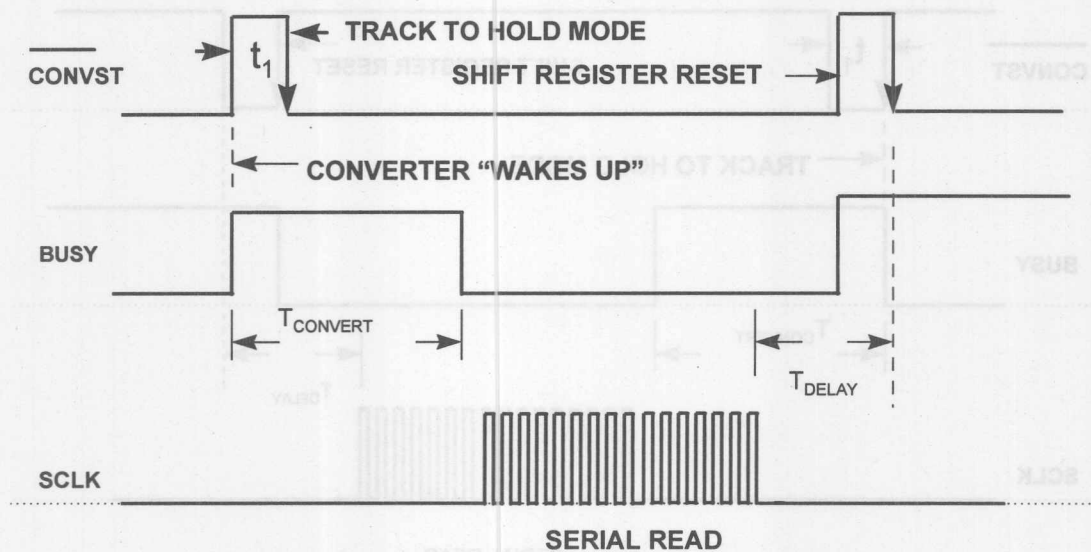


Normal (High Performance) Mode

3 - 49



Auto Power Down Feature (con't)



Automatic "Sleep" (Power Down) Mode

3 - 50



AD7816, AD7817 and AD7818 1/4-Channel 10-Bit ADCs w/ On-Board Temp Sensor

- **100 ksps Throughput**
- **Input Channels :**
 - **AD7817 : 4 Channel**
 - **AD7818 : 1 Channel**
 - **AD7816 : Temp Sensor, Only**
- **On-Chip Temp Sensor :**
 - **0.25 deg C Resolution**
 - **± 1 deg C Error from -40 deg C to + 80 deg C**
 - **± 2 deg C Error from -55 deg C to + 125 deg C**

3 - 51



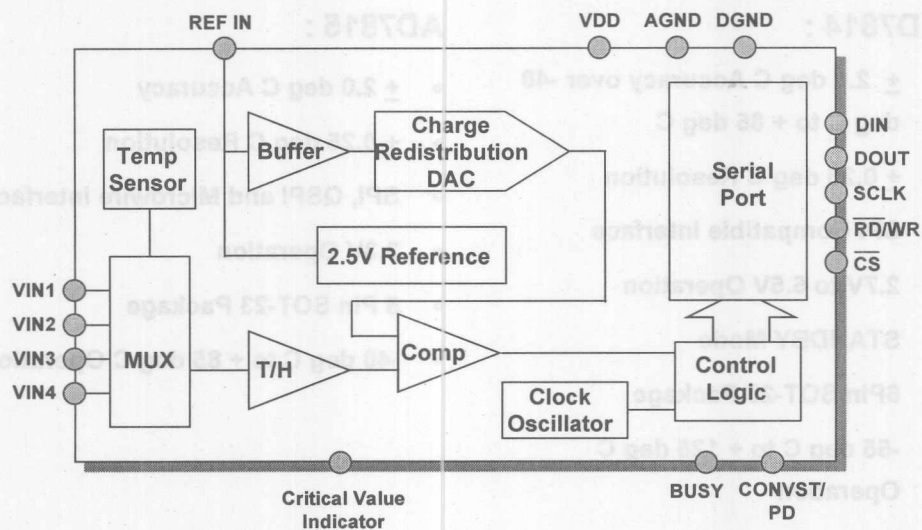
AD7816, AD7817 and AD7818 (con't)

- **On-Chip 2.5V Reference, $\pm 1\%$**
- **“Over Temperature” Indicator**
- **Low Power Performance :**
 - **560 uW @ 50 ksps Throughput**
 - **Sleep Mode : 3 uW max**
- **Flexible DSP/Microcontroller Serial Interface**
- **Power Down Mode W/ Data Readout During Powerdown**
- **Package Styles :**
 - **AD7817 : 16 Pin SOIC and TSSOP**
 - **AD7816, AD7818 : 8 Pin SOIC and MicroSOIC**

3 - 52



AD7817 - Block Diagram



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Preliminary
Information

AD7814* and AD7815* 10 Bit Digital Temperature Sensors

AD7814 :

- ± 2.0 deg C Accuracy over -40 deg C to + 85 deg C
- ± 0.25 deg C Resolution
- SPI Compatible Interface
- 2.7V to 5.5V Operation
- STANDBY Mode
- 6Pin SOT-23 Package
- -55 deg C to + 125 deg C Operation

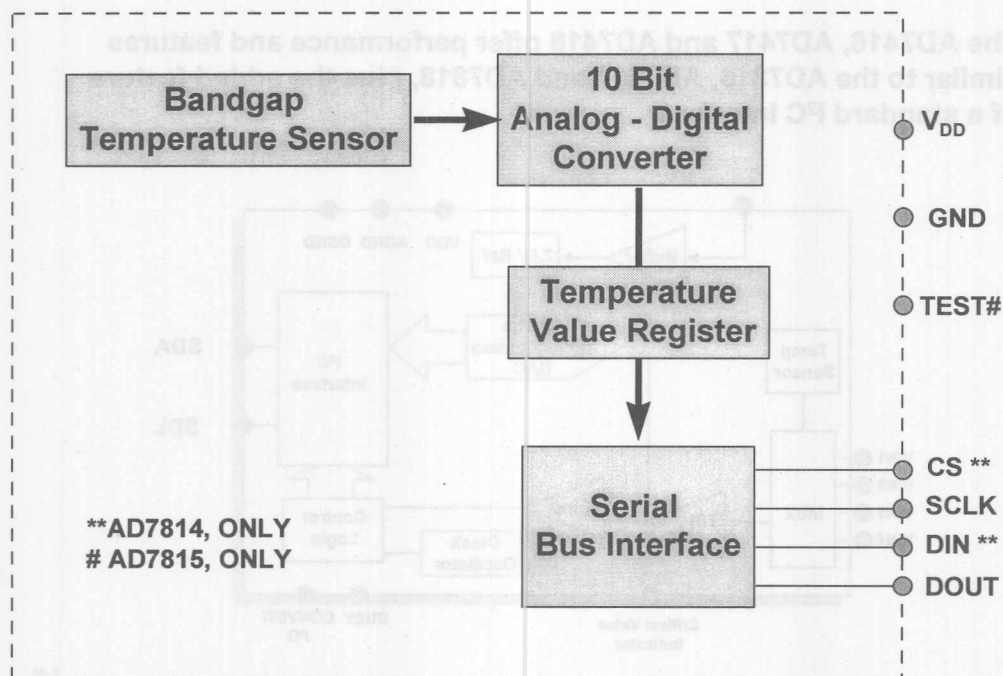
AD7815 :

- ± 2.0 deg C Accuracy
- ± 0.25 deg C Resolution
- SPI, QSPI and Microwire Interface
- 3.3V Operation
- 5 Pin SOT-23 Package
- -40 deg C to + 85 deg C Operation

3 - 54



AD7814, AD7815 - Simplified Diagram



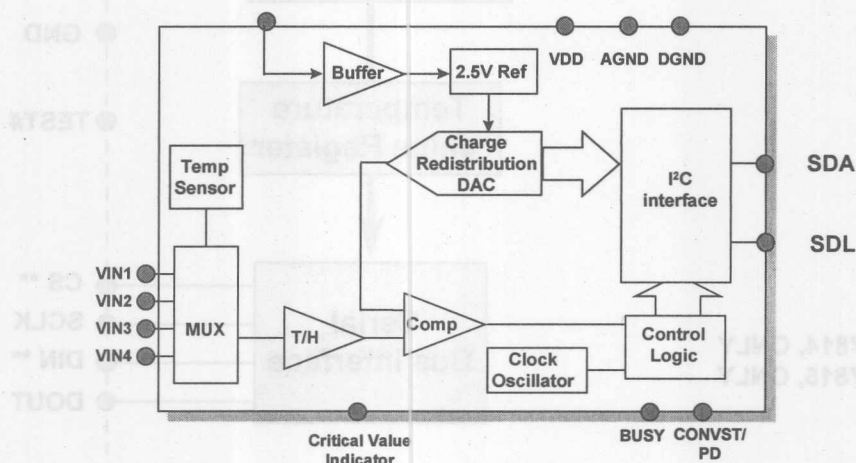
3 - 55



Preliminary
Information

AD7416, AD7417* and AD7418* 1/4-Channel 10-Bit ADCs w/ On-Board Temp Sensor

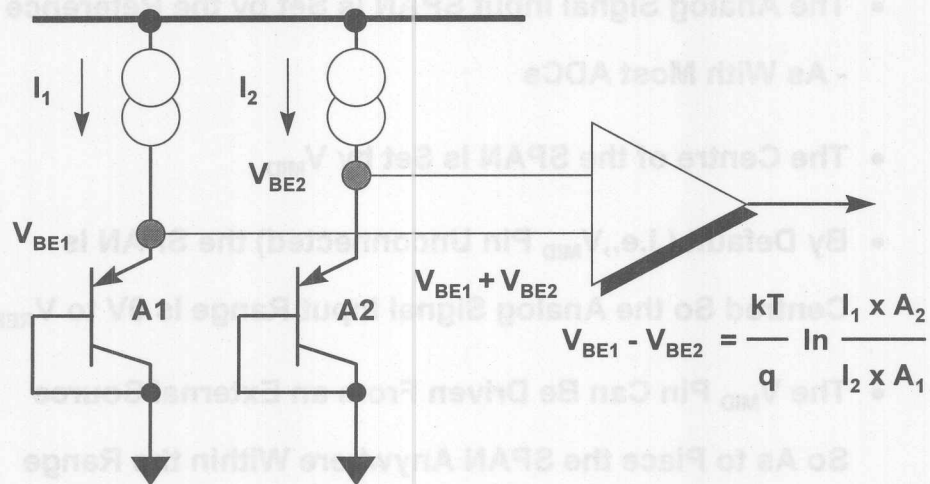
The AD7416, AD7417 and AD7418 offer performance and features similar to the AD7816, AD7817 and AD7818, plus the added feature of a standard I²C Interface



3-56



The On-Chip Temperature Sensor



3 - 57



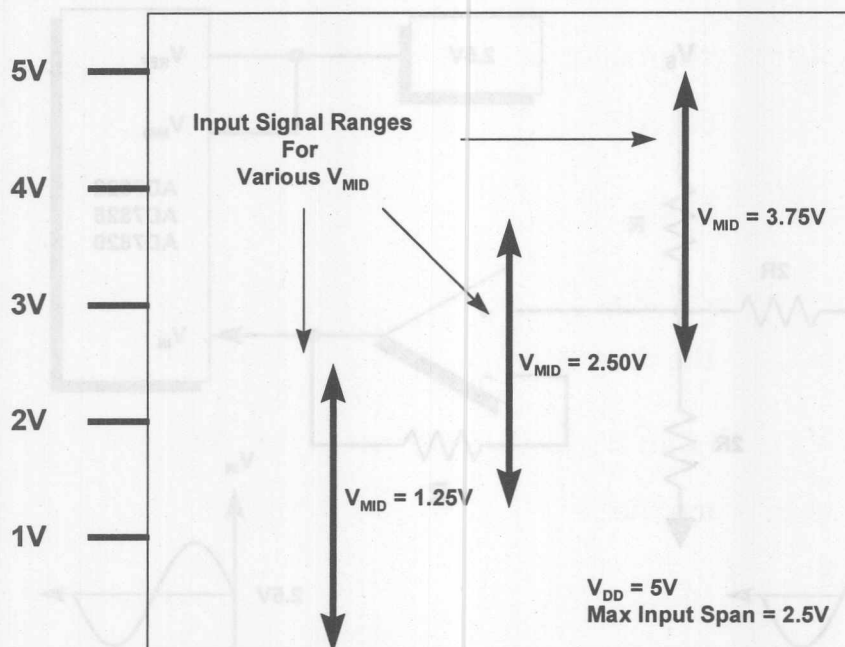
Analog Input Adjustments

- **The Analog Signal Input SPAN Is Set by the Reference**
 - **As With Most ADCs**
- **The Centre of the SPAN Is Set by V_{MID}**
- **By Default (,i.e., V_{MID} Pin Unconnected) the SPAN Is Centred So the Analog Signal Input Range Is 0V to V_{REF}**
- **The V_{MID} Pin Can Be Driven From an External Source So As to Place the SPAN Anywhere Within the Range 0V to V_{DD} .**

3 - 58



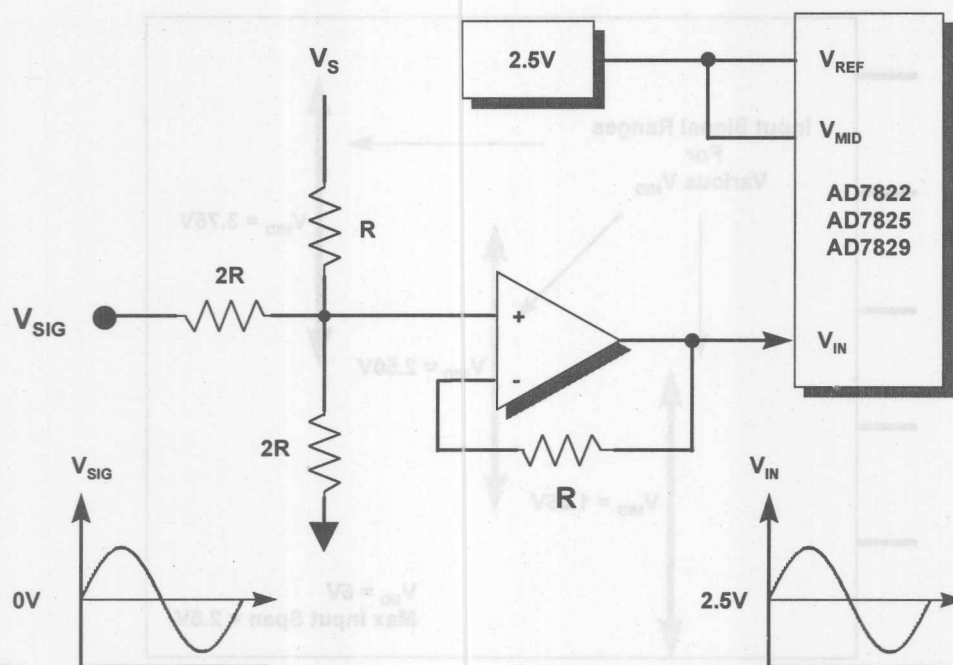
The SPAN Can Be Set Anywhere Within the Range of V_{DD}



3 - 59



How V_{MID} Might Be Used...Accommodating Bipolar Inputs



3 - 60



**Preliminary
Information**

AD747X* Series 10/12 Bit A/D Converters

**The AD747X Series of Successive Approximation A/D Converters Represent
A Major Breakthrough in High Speed Low Power Performance!**

- ***x10 Improvement in Power/Throughput Ratio***
- ***Fastest ADI SAR A/D Converters***
- ***ADI's Only 3V >1MSPS A/D Converter***
- ***Parallel & Serial Versions***
- ***Serial 1.75MSPS A/D Converter***
- ***Proprietary Power Management Scheme***

3-61



Compare the Performance of the AD747X Series to ADI's popular AD785X and AD789X Series...

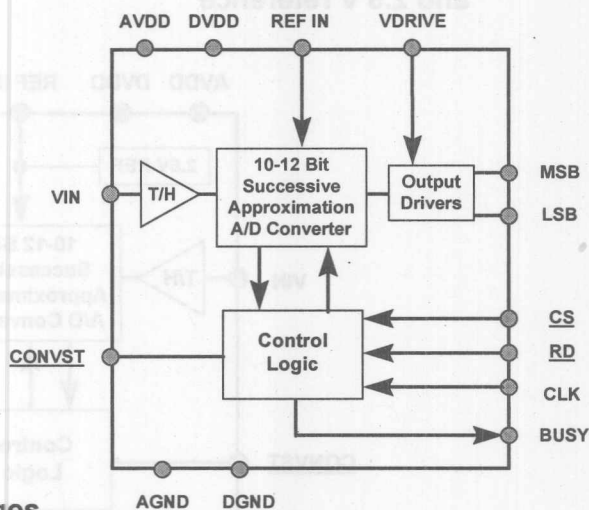
	AD747X	AD785X	AD789X
<i>Faster Throughput</i>	0.5 – 2.0 MSPS	200 ksps	600 ksps
<i>Wider Input BW</i>	500 kHz	10 kHz	100 kHz
<i>Lower Power</i>	11 mW	30 mW	90 mW
<i>Faster Bus Interface</i>	25 ns	55 ns	35 ns



***Preliminary**

AD7470* - AD7472* 10/12 Bit, Parallel A/D Converters

- **Fast Throughput :**
 - AD7470 : 10 bit, 2 MSPS
 - AD7471 : 12 bit, 500 ksps
 - AD7472 : 12 bit, 1.75 MSPS
- 70 dB SNR @ 500 kHz
- V_{dd} from 2.7 V to 5.25 V
- Low Power : 3 mW , typ
- Shutdown Mode : 1 μ A max
- 24 Pin SOIC and TSSOP Packages



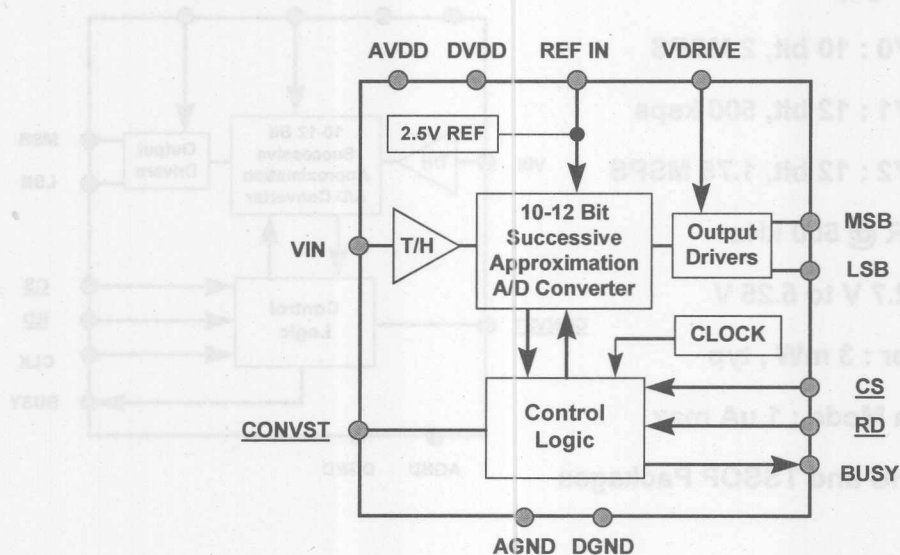
3 - 63



**Preliminary*

AD7492* 12 Bit, 1.75 MSPS Parallel A/D Converter

The AD7492 is an AD7472 with the addition of an internal clock and 2.5 V reference



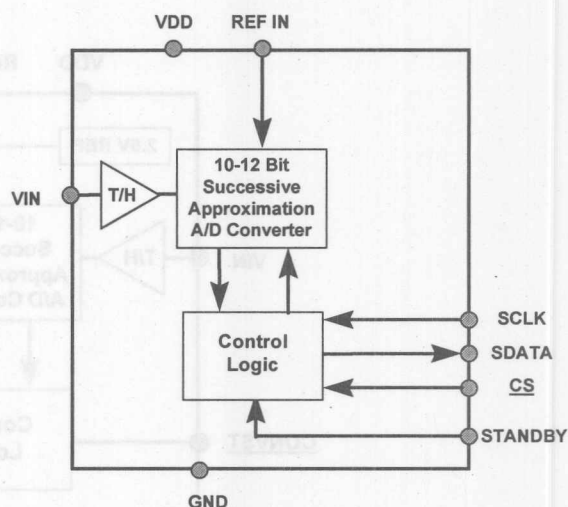
3-64



**Preliminary*

AD7474* and AD7475* 12 Bit, Serial A/D Converters

- Fast Throughput :
 - AD7474 : 12 bit, 500 ksps
 - AD7475 : 12 bit, 1.75 MSPS
- 70 dB SNR @ 500 kHz
- V_{dd} from 2.7 V to 5.25 V
- Low Power : 3 mW , typ
- Shutdown Mode : 1 μ A max
- 8 Pin SOIC and μ SOIC Packages



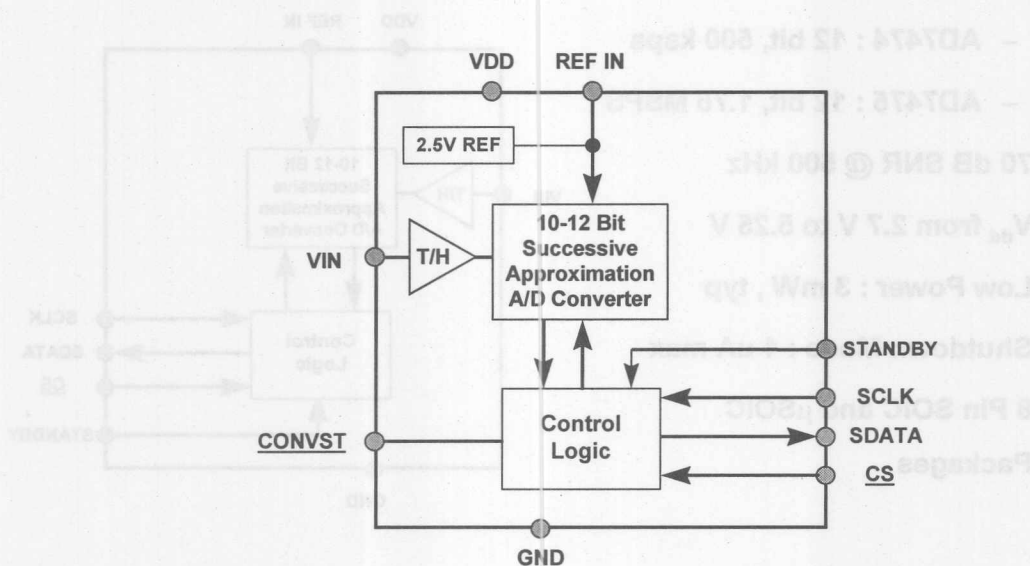
3 - 65



*Preliminary

AD7495* 12 Bit, 1.75 MSPS Serial A/D Converter

The AD7495 is an AD7475 with the addition of an on-board 2.5 V reference



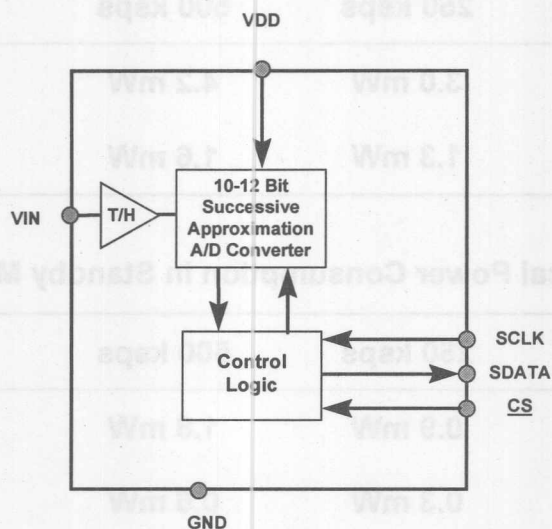
3-66



**Preliminary*

AD7476* 12 Bit, 1.0 MSPS Serial A/D Converter

The AD7476 is similar in performance to the AD7473-AD7475 and is offered in a compact 6 pin SOT-23 package.



3-67



Power Consumption vs Clock Rate

Typical Power Consumption in Normal Mode

Clock Rate	250 ksps	500 ksps	1 Msps
5V Supply	3.0 mW	4.2 mW	6.5 mW
3V Supply	1.3 mW	1.6 mW	2.4 mW

Typical Power Consumption in Standby Mode

Clock Rate	250 ksps	500 ksps	1 Msps
5V Supply	0.9 mW	1.8 mW	3.6 mW
3V Supply	0.3 mW	0.6 mW	1.2 mW

3 - 68



ADI's AD788X Family of 12 Bit A/D Converters Feature...

- **Wide Selection of Input Ranges :**
 - **+ 2.5V, + 5V, or + 10V**
 - **$\pm 2.5V$, $\pm 5V$, or $\pm 10V$**
- **Single +5V Supply Operation**
- **Power Down or SLEEP mode**
- **Overvoltage Protection up to $\pm 20V$**

3-69



Preliminary
Information

AD7887*, AD7888*

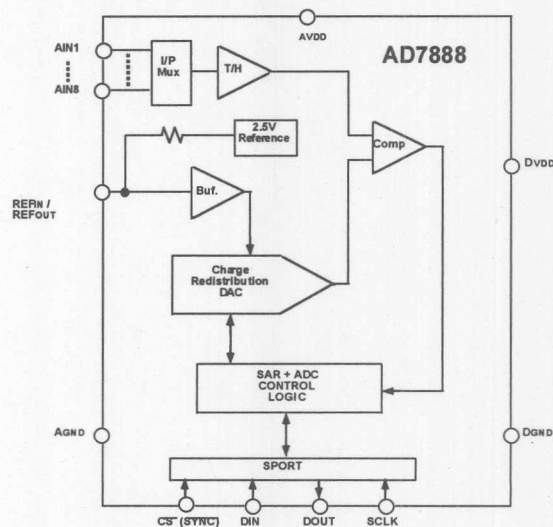
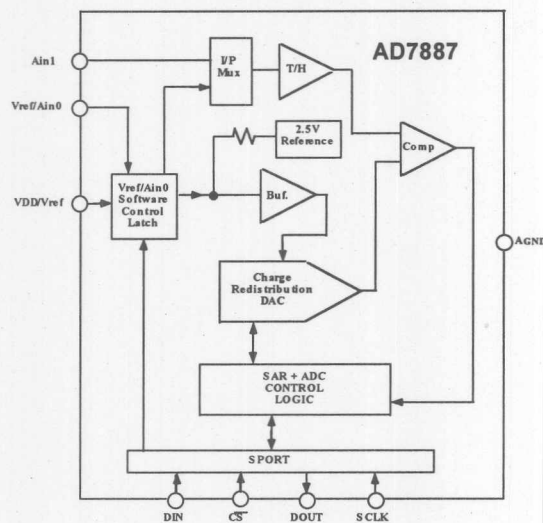
12 Bit, 200 ksps, 2/8 Channel, Serial A/D Converters

- Specified for V_{DD} of 2.7V to 5.25V
 - 700 μ A max @ 200ksps
 - 450 μ A max @ 100ksps
 - Shut-Down Mode: 1 μ A max
- One/Two Single-Ended Inputs (AD7887)
- Eight Single-Ended Inputs (AD7888)
- Analog Input Range: 0V to VREF (VDD)
- SPI, QSP AND μ Wire-Compatible Serial Interface:
- 3 MHz Full Power Bandwidth
- 8-pin Narrow SOIC and μ SOIC Packages (AD7887)
- 16-pin Narrow SOIC and TSSOP Packages (AD7888)

3 - 70



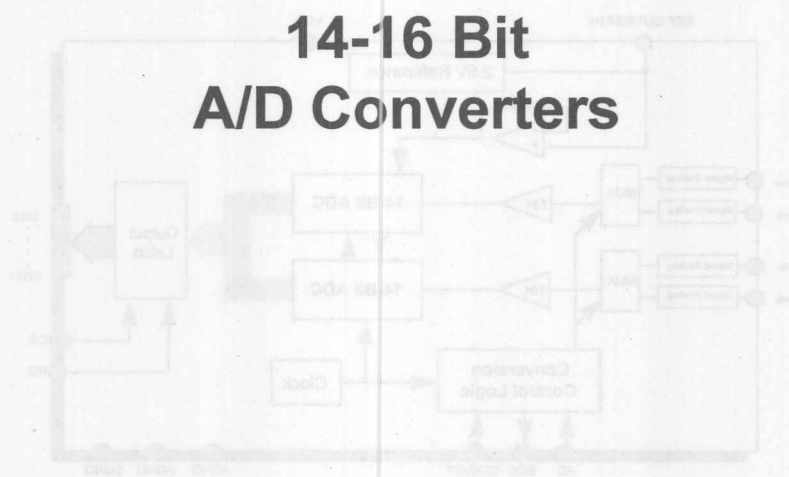
AD7887, AD7888







14-16 Bit A/D Converters



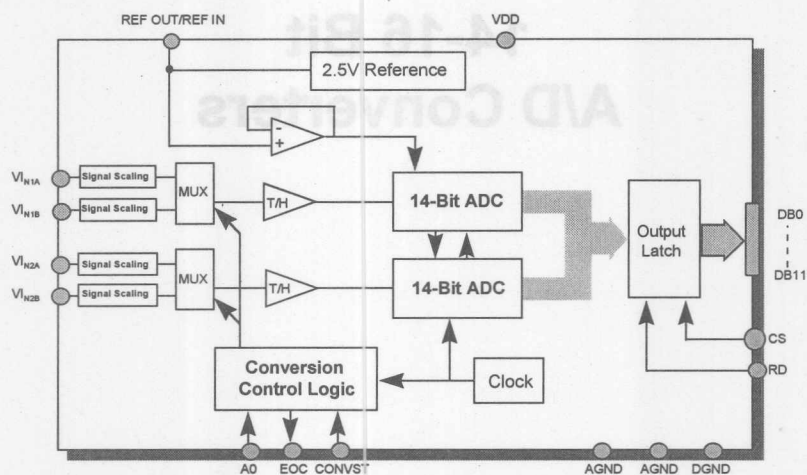
3-73



AD7863

Dual Channel, Simultaneous Sampling A/D Converters

The AD7863 14 Bit, 200 kps A/D Converter provides simultaneous sampling and conversion of 2 phase-related or time-related signals. It also has a 2-channel multiplexer on each input, giving a total of 4 input channels.

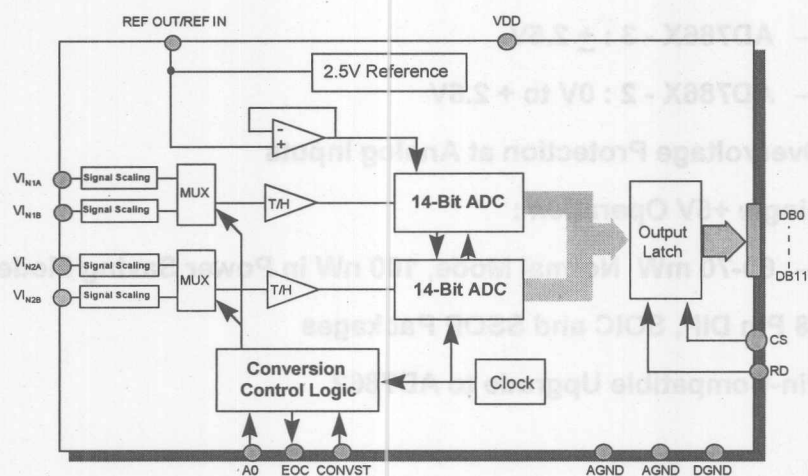


3-74



AD7863 - Simplified Diagram

The AD7863 is primarily designed for, but not limited to, motor control applications, such as AC servos and Inverters. The 2-channels of simultaneous sampling are used to control the two currents (3rd current is calculated) in a 3-phase system.



3-75



AD7863 - Key Specs and Features

- Two (2) 14-bit ADC's with 4.5 us Conversion Times
- Selection of Input Ranges :
 - AD786X - 10 : $\pm 10V$
 - AD786X - 3 : $\pm 2.5V$
 - AD786X - 2 : 0V to + 2.5V
- Overvoltage Protection at Analog Inputs
- Single +5V Operation :
 - 60-70 mW Normal Mode, 100 nW in Power Saving Mode
- 28 Pin DIP, SOIC and SSOP Packages
- Pin-Compatible Upgrade to AD7862

3 - 76



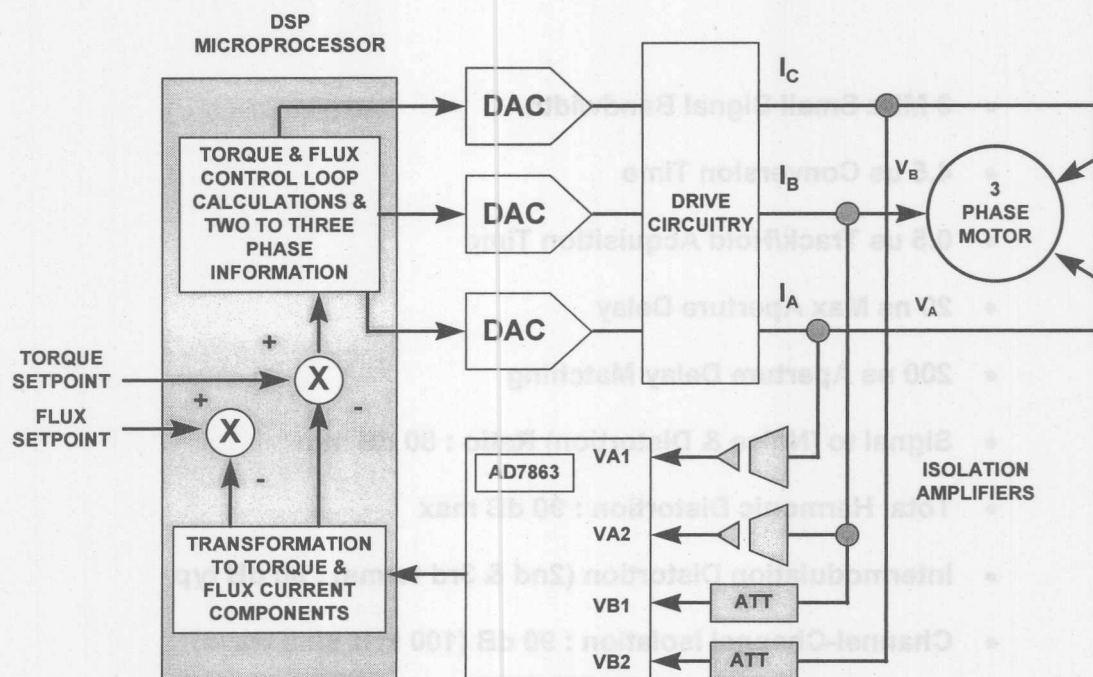
AD7863 Dynamic Performance

- 3 MHz Small Signal Bandwidth
- 4.5 μ s Conversion Time
- 0.5 μ s Track/Hold Acquisition Time
- 20 ns Max Aperture Delay
- 200 ns Aperture Delay Matching
- Signal to (Noise & Distortion) Ratio : 80 dB min
- Total Harmonic Distortion : 90 dB max
- Intermodulation Distortion (2nd & 3rd terms) : 90 dB typ
- Channel-Channel Isolation : 90 dB (100 kHz sine wave)

3-77



Vector Motor Control Using the AD7863



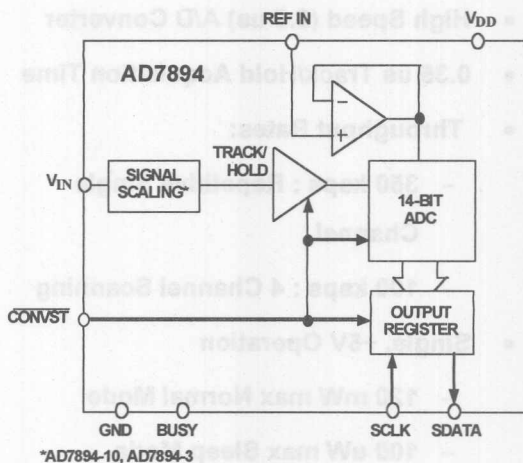
3-78



AD7894 5V, 14 Bit Serial Bipolar A/D Converter

The AD7894 provides bipolar operation and serial output in a compact 8 pin SOIC package!

- 4.5 us Conversion Time
- On-Chip Track/Hold
- Selection of Input Ranges:
 - AD7894 -10 : $\pm 10V$
 - AD7894-3 : $\pm 2.5V$
 - AD7894-2 : 0V to 2.5V
- High Speed Serial Interface
- Single Supply, Low Power Operation : 5V @ 20 mW



3-79



Preliminary
Information

AD7865*

14 Bit, 4 Channel, Simultaneous Sampling A/D Converter

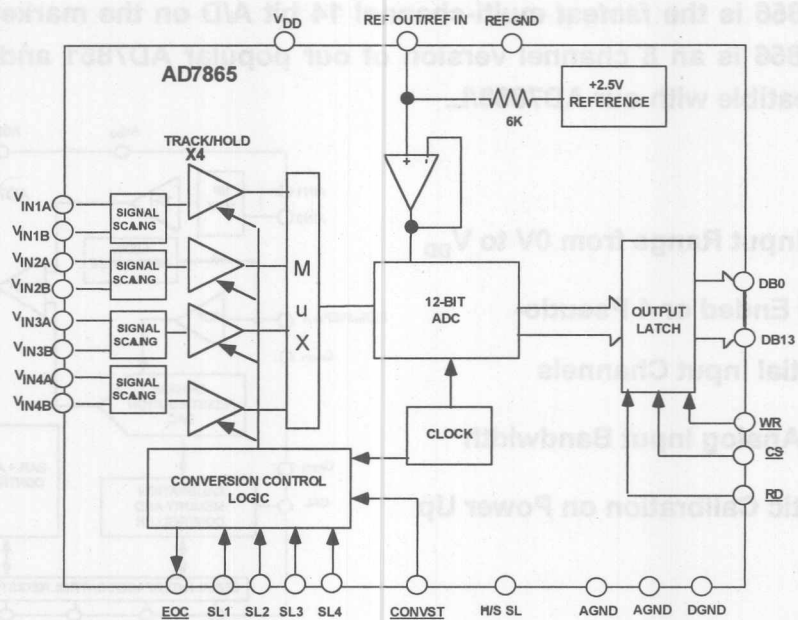
Simultaneous sampling preserves the relative phase/timing relationships of each input signal.

- High Speed (2.5 μ s) A/D Converter
- 0.35 μ s Track/Hold Acquisition Time
- Throughput Rates:
 - 350 ksps : Repetitive Single Channel
 - 100 ksps : 4 Channel Scanning
- Single, +5V Operation
 - 120 mW max Normal Mode
 - 100 μ W max Sleep Mode
- Analog Input Ranges : ± 5 V, ± 10 V
- High Speed Parallel Interface
- ± 20 Volts Overvoltage Protection on Analog Inputs
- 44 Pin PQFP Package

3 - 80



AD7865 - Block Diagram



3 - 81

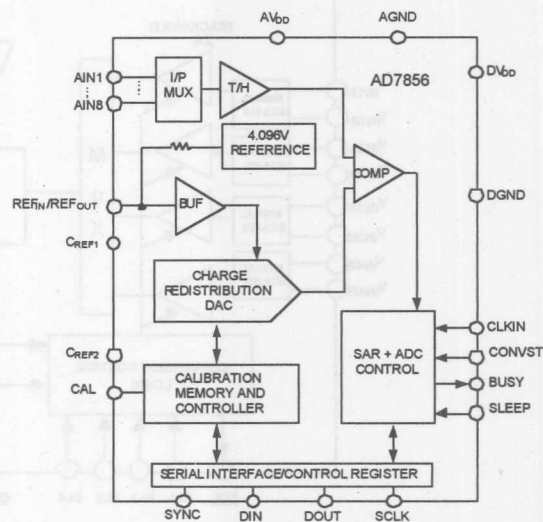


AD7856

14 Bit, 8 Channel 285 kbps Sampling A/D Converter

The AD7856 is the *fastest* multi-channel 14 bit A/D on the market today! The AD7856 is an 8 channel version of our popular AD7851 and is also pin-compatible with our AD7858/L..

- Analog Input Range from 0V to V_{DD}
- 8 Single Ended or 4 Pseudo-Differential Input Channels
- 10 MHz Analog Input Bandwidth
- Automatic Calibration on Power Up

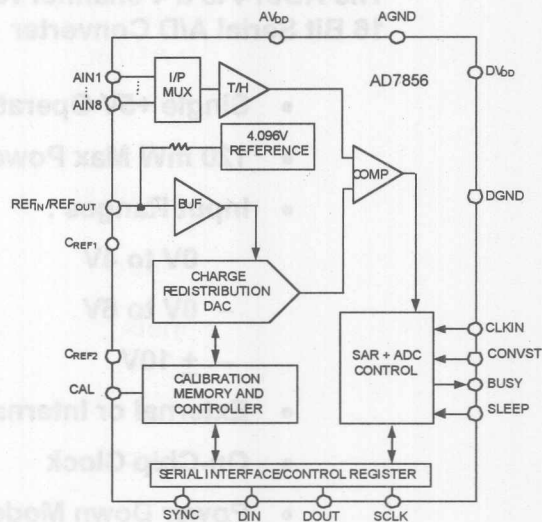


3-82



AD7856 - Key Specs and Features (con't)

- Self and System Calibration
- Automatic Power Down After Conversion (typ 52 μ W)
- Versatile Serial I/O Port :
8051/SPI/QSPI/uP Compatible
- Single +5V Power Supply, 60 mW typical
- 24 Pin DIP, SOIC and SSOP Packages



3 - 83



AD974

16 Bit, 150 ksps, 4 Channel A/D Converter

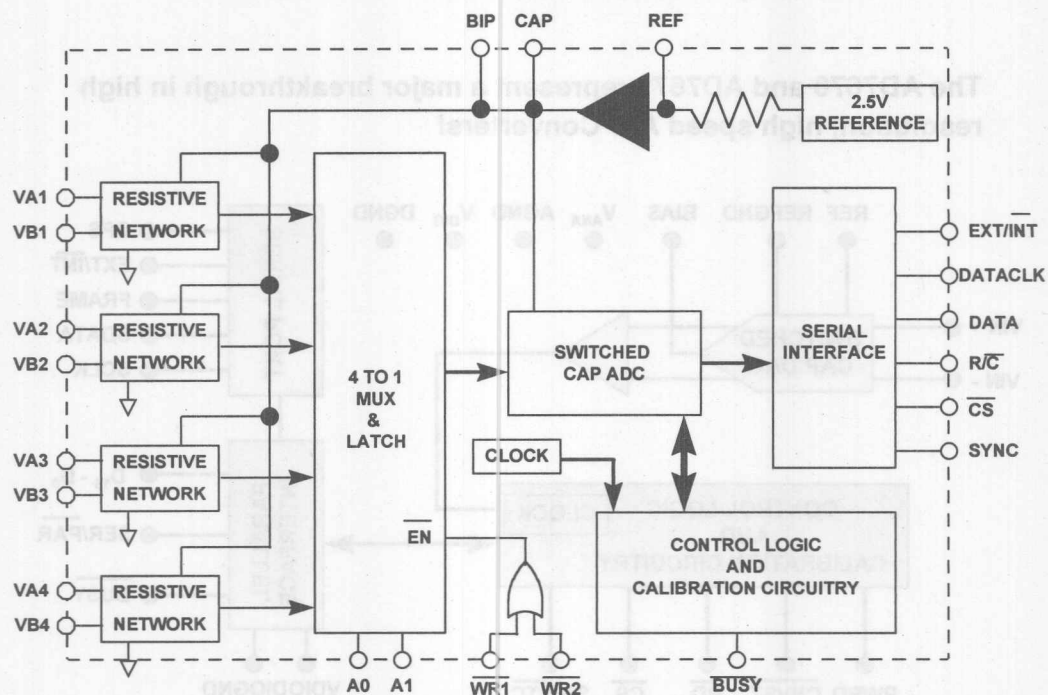
The AD974 is a 4 channel version of our AD977/AD977A
16 Bit Serial A/D Converter



- Single +5V Operation
- 120 mW Max Power Dissipation
- Input Ranges :
 - 0V to 4V
 - 0V to 5V
 - $\pm 10V$
- External or Internal 2.5V Reference
- On-Chip Clock
- Power Down Mode

3-84

AD974 - Simplified Diagram

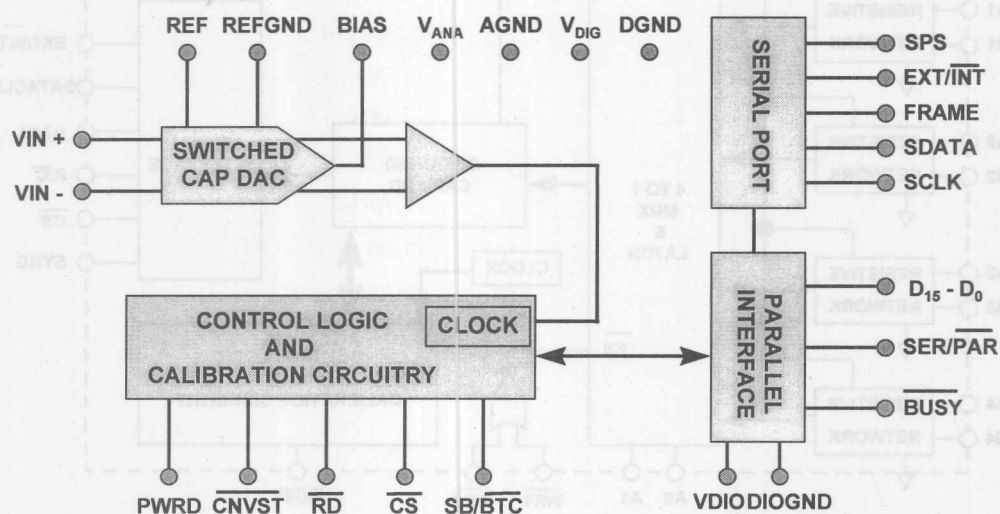


3 - 85



AD7670*, AD7671* 16 Bit, 1 MHz CMOS A/D Converters

The AD7670 and AD7671 represent a major breakthrough in high resolution, high speed A/D Converters!



3-86



AD7670, AD7671 : Key Specs and Features

The AD7670, AD7671 employ a charge redistribution, successive approximation A/D Converter architecture to eliminate the latency found in multi-stage A/D Converters.

- **Analog Input Range :**
 - AD7670 : 0V to 2.5V
 - AD7671 :
- **DC Performance :**
 - ± 1.5 LSB Max INL
 - No Missing Codes to 16 Bits
- **Dynamic Performance ($F_{in} = 100$ kHz) :**
 - Signal to Noise and Distortion (SINAD) : 90 dB
 - Total Harmonic Distortion : 96 dB
- **Selectable Conversion Speeds :**
 - WARP (High Speed) Mode : 1.33 MHz
 - IMPULSE (Low Power) Mode : 1 MHz
- **Single +5V Operation**
 - 250 mW max
- **44 Pin PQFP Package**
- **- 40 deg C to + 85 deg C Operation**

3 - 87



AD9260

16 Bit, Oversampling A/D Converter

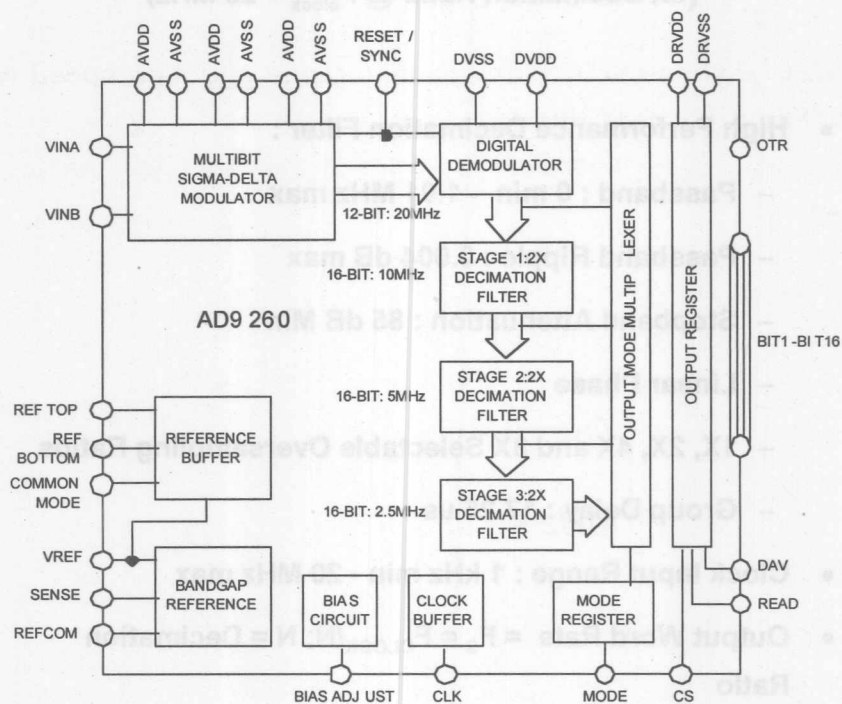
The AD9260 provides both wide dynamic range and high speed with an oversampling ratio of 8X through the use of a proprietary new technique which combines the advantages of sigma-delta and pipeline converter technologies!

- **16 Bit Resolution**
- **8X Oversampling**
- **20 MHz Clock**
- **2.5 MHz Output Word Rate!**

3 - 88



AD9260 Block Diagram



3-89



AD9260 - Key Specs and Features

(8X Decimation Ratio @ $F_{\text{clock}} = 20 \text{ MHz}$)

- High Performance Decimation Filter :
 - Passband : 0 min - 1.01 MHz max
 - Passband Ripple : 0.004 dB max
 - Stopband Attenuation : 85 dB Min
 - Linear Phase
 - 1X, 2X, 4X and 8X Selectable Oversampling Ratios
 - Group Delay : 17.25 us
- Clock Input Range : 1 kHz min - 20 MHz max
- Output Word Rate = $F_s = F_{\text{CLOCK}}/N$; N = Decimation Ratio

3 - 90



AD9260 - Key Specs and Features

N = 8 (con't)

- **Dynamic Performance ($F_{IN} = 100$ kHz):**
 - **Signal-to-Noise Ratio : 89 dB**
 - **Total Harmonic Distortion : -98 dB**
 - **Spurious-Free Dynamic Range : 100 dB**
 - **Input Referred Noise : 0.6 dB**
- **Single +5V Analog Supply, +5V/+3V Digital Supply**
 - **550 mW @ 2.5 MHz Data Rate**
 - **< 150 mW @ Reduced Clock Rates**
- **Synchronize Capability for Parallel ADC Interface**
- **Two's Complement Output Format**
- **44 Pin MQFP Package**

3 - 91



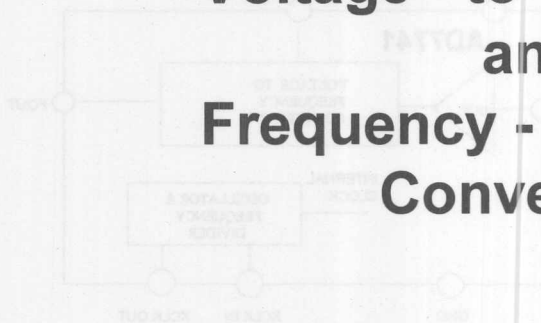
AD9280 - Key Specs and Features N = 8 (cont)

- Dynamic Performance ($F_{IN} = 100 \text{ kHz}$):
 - Signal-to-Noise Ratio : 83 dB
 - Total Harmonic Distortion : -88 dB
 - Spurious-Free Dynamic Range : 100 dB
 - Input Referred Noise : 0.6 dB
- Single +5V Analog Supply, +1V/+3V Digital Supply
 - 880 mW @ 2.5 MHz Data Rate
 - < 180 mW @ Reduced Clock Rates
- Synchronizes Capability for Parallel ADC Interface
- Two's Complement Output Format
- 44 Pin MFP Package

3 - 92



Voltage - to - Frequency and Frequency - to - Voltage Converters



- Input Signal
- 5 MHz Output Frequency
- External 5 MHz
- Internal Clock Oscillator
- Single 5V Operation
- 8-Pin DIP and SOIC Packages

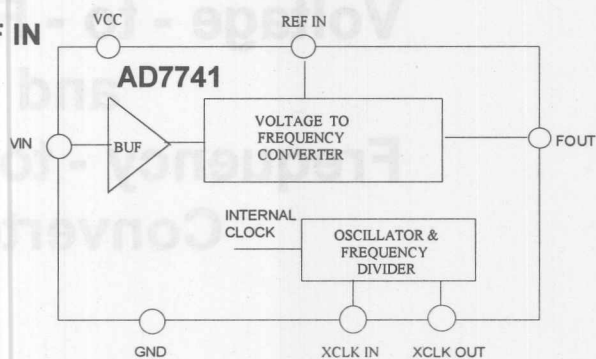
3 - 93



Preliminary
Information

AD7741* 5 MHz Voltage - Frequency Converter

- Input Signal Range : 0V to REF IN
- 5 MHz Output Frequency
- External 2.5V Reference
- Internal Clock Oscillator
- Single 5V Operation
- 8-Pin DIP and SOIC Packages



3-94



Preliminary
Information

AD7742*

5 MHz Dual Channel Voltage-Frequency Converter

- Unipolar/Bipolar Input Ranges :

- REF IN or REF IN/2

- \pm REF IN or \pm REF IN/2

- 5 MHz Min Output Frequency

- On-Chip 2.5V Reference

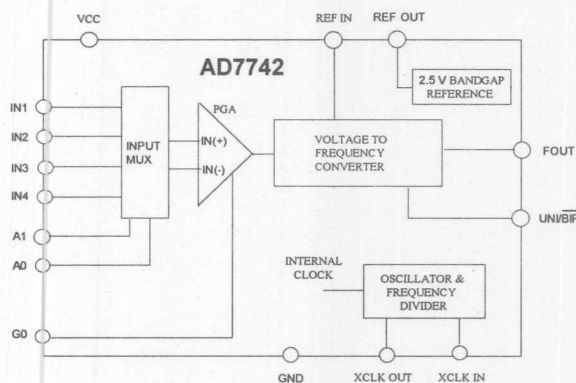
- External 2.5V Reference

- Common Mode range from

- 0.4 V to +3 V

- Single 5V Operation

- 16 Pin DIP & SOIC Packages



3 - 95



- 16 Pin DIP & SOIC Packages
- Single 5V Operation
- -0.4 V to +2 V
- Common Mode range from
- External 2.5V Reference
- On-Chip 2.5V Reference
- 5 kHz Min Output Frequency
- \pm REF IN or \pm REF IN2
- - REF IN or REF IN2
- Unipolar/Bipolar Input Ranges :



Sigma-Delta (Σ - Δ) A/D Converters

3 - 97



What is a Sigma-Delta Converter?

A Sigma-Delta Converter Uses Oversampling Plus Digital Filtering to Achieve Very High Resolution (18-24 Bits) at Only A Moderate Cost.

3 - 98



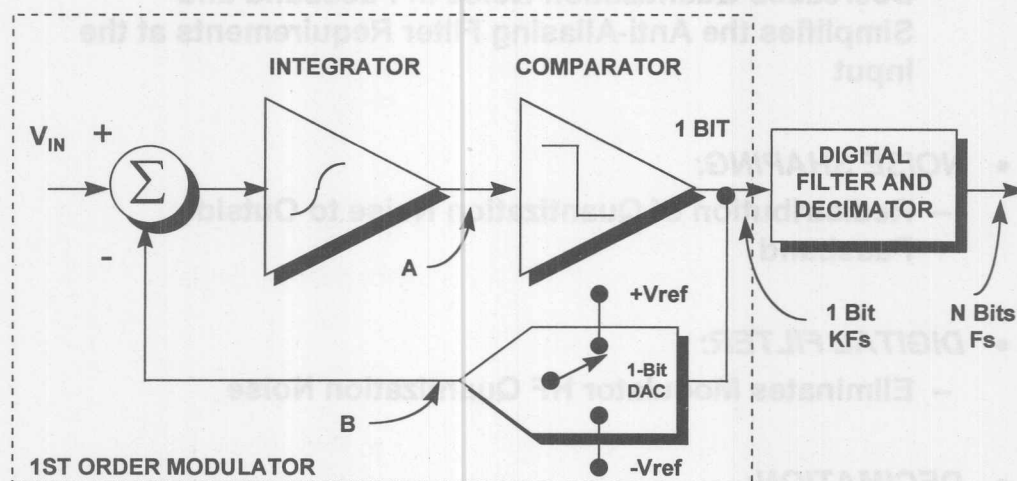
Basic Elements of the Sigma-Delta Converter...

- **OVERSAMPLING:**
 - Decreases Quantization Noise in Passband and Simplifies the Anti-Aliasing Filter Requirements at the Input
- **NOISE SHAPING:**
 - Redistribution of Quantization Noise to Outside Passband
- **DIGITAL FILTER:**
 - Eliminates Modulator HF Quantization Noise
- **DECIMATION:**
 - Reduces Output Data Rate

3 - 99



A Sigma-Delta A/D Converter



3 - 100



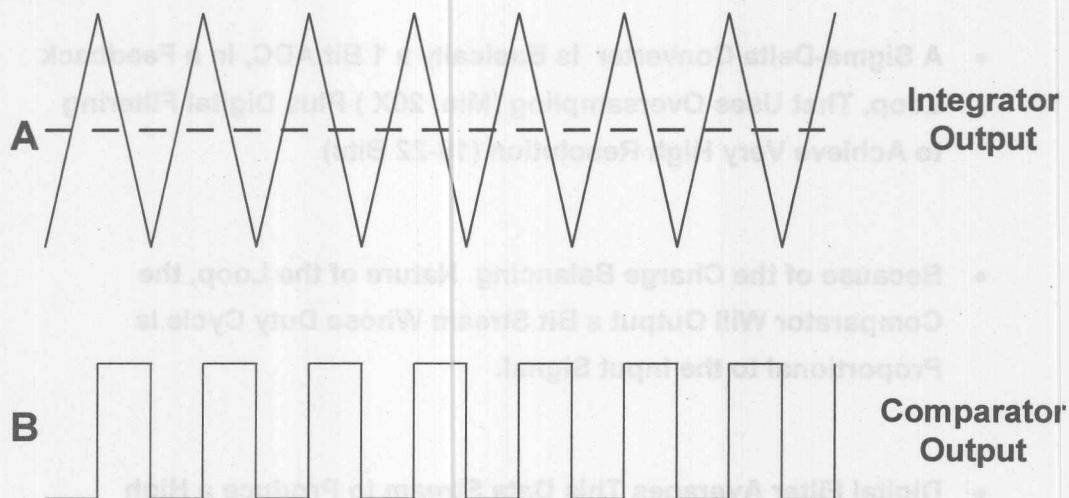
A Sigma-Delta A/D Converter (con't)

- **A Sigma-Delta Converter Is Basically a 1 Bit ADC, in a Feedback Loop, That Uses Oversampling (Min. 20X) Plus Digital Filtering to Achieve Very High Resolution (18-22 Bits)**
- **Because of the Charge Balancing Nature of the Loop, the Comparator Will Output a Bit Stream Whose Duty Cycle Is Proportional to the Input Signal.**
- **Digital Filter Averages This Data Stream to Produce a High Resolution Output.**

3 - 101



Sigma-Delta Modulator Waveforms...

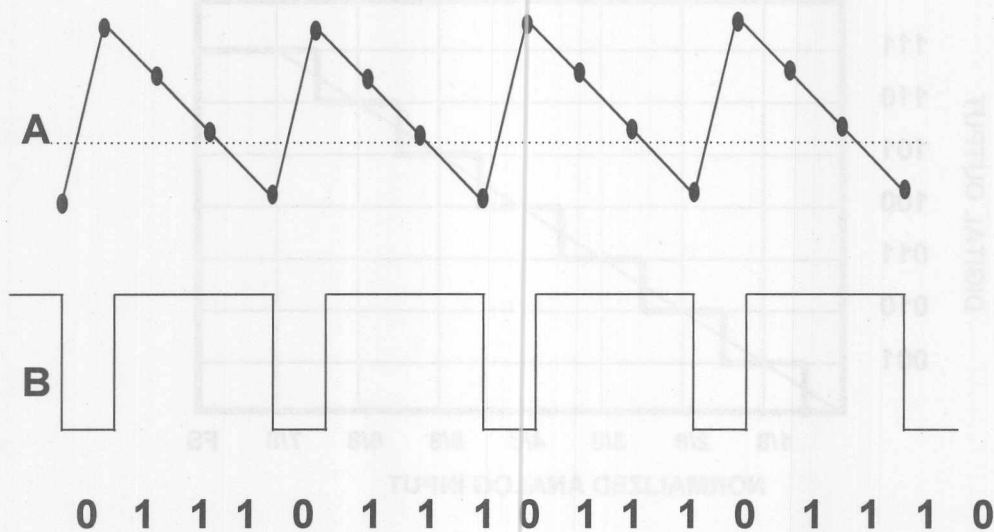


$V_{in} = 0V$ or Midscale

3 - 102



Sigma-Delta Modulator Waveforms (con't)

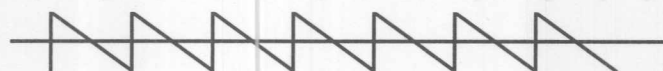
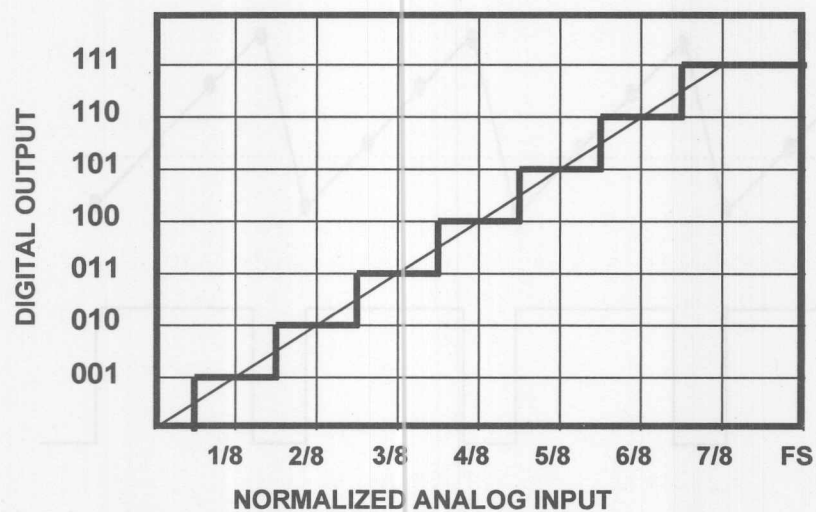


$V_{in} = V_{ref}/2$ or $3/4$ Span

3-103



A Review of Quantization Noise



quantization noise error

3-104



Some Useful Equations from Quantization Theory

- Q is the size of the LSB
- The RMS value of the Quantization noise (sawtooth) is its peak value Q/2 divided by square root 3, or $Q/\sqrt{12}$
- Full-scale Sinewave RMS Signal to RMS noise ratio in the Nyquist Bandwidth for an N-bit ADC,

$$\text{SNR} = 6.02N + 1.76\text{dB}$$

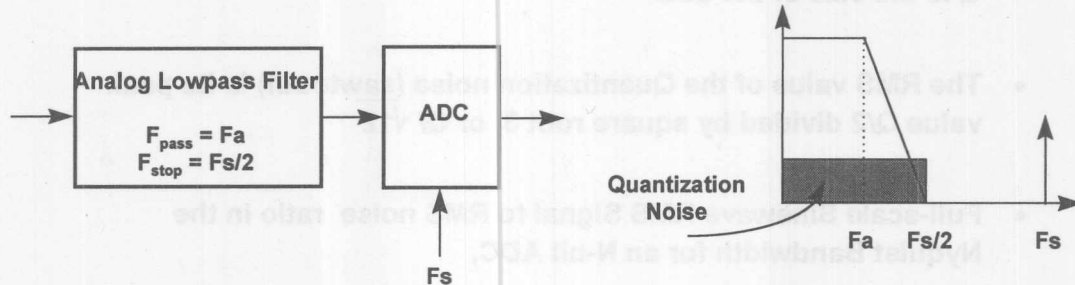
- Effective Number of Bits (ENOB) equals, -

$$\text{ENOB} = \frac{\text{SNR}_{\text{actual}} - 1.76\text{dB}}{6.02}$$

3 - 105



Sampling and the Nyquist Bandwidth...

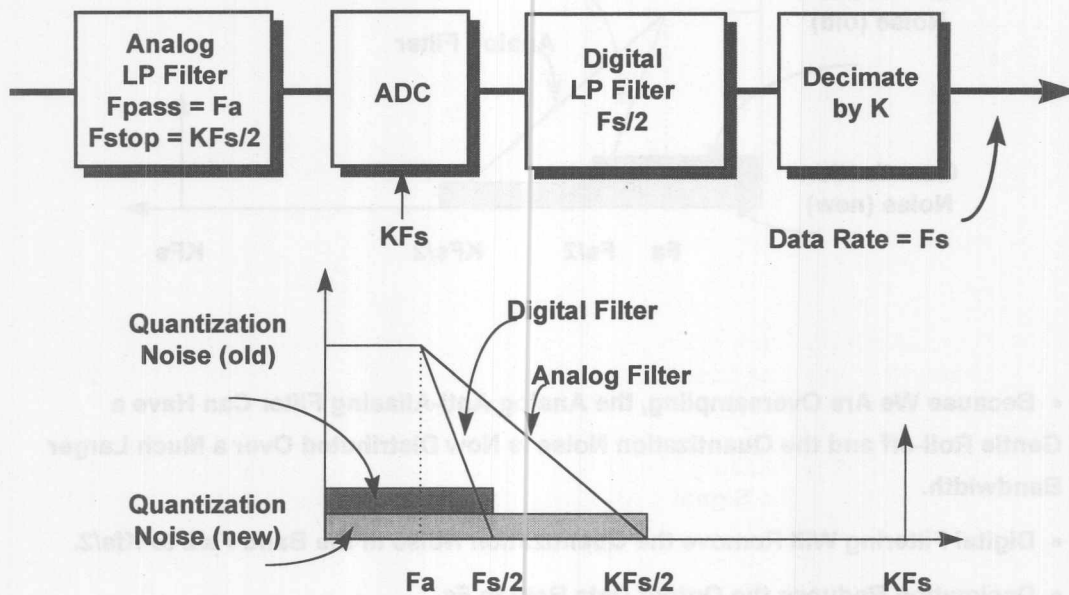


- The Nyquist Sampling Theory Demands That the Bandwidth of the Sampled Signal Be Less Than Half the Sampling Frequency to Prevent a Phenomenon Known As Aliasing.
- Using an “Anti-Aliasing” Filter, We Band-Limit the Input-Signal So That the Attenuation of the Signal Is Greater Than the Required Dynamic Range at $F_s/2$.
- The Quantization Noise Is Spread Evenly Over $F_s/2$.

3 - 106



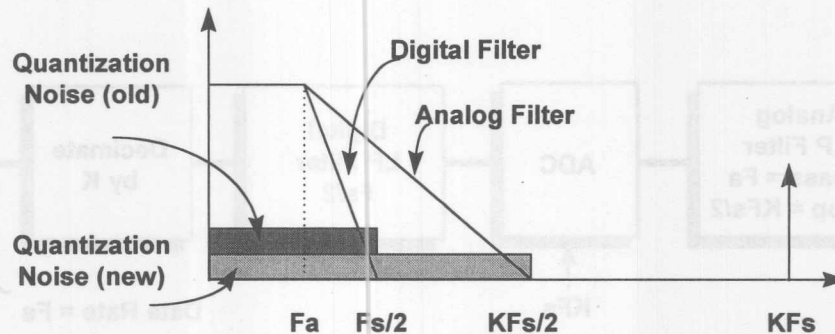
Oversampling...



3 - 107



Oversampling (con't)

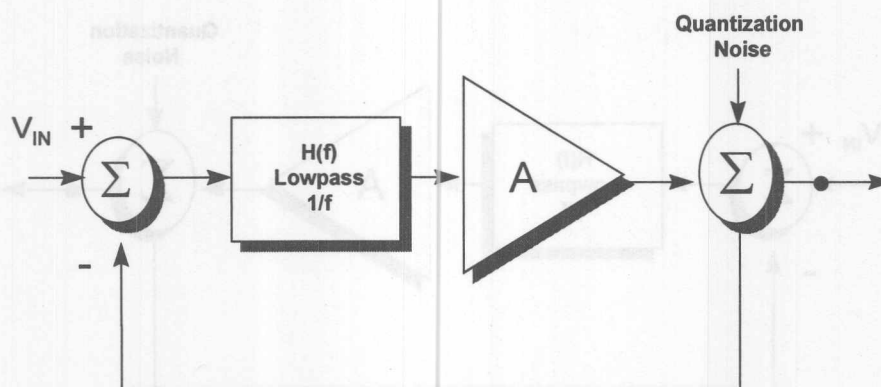


- Because We Are Oversampling, the Analog Anti-Aliasing Filter Can Have a Gentle Roll-off and the Quantization Noise Is Now Distributed Over a Much Larger Bandwidth.
- Digital Filtering Will Remove the Quantization Noise in the Band $F_s/2$ to $Kf_s/2$.
- Decimation Reduces the Output Data Rate to F_s .

3 - 108



Noise Shaping



We approximate the integrator to a lowpass filter with a response of $1/f$. We can approximate the comparator to a gain of 1 followed by a quantization noise injector. This yields, -

$$Y = (x-y)/f + q$$

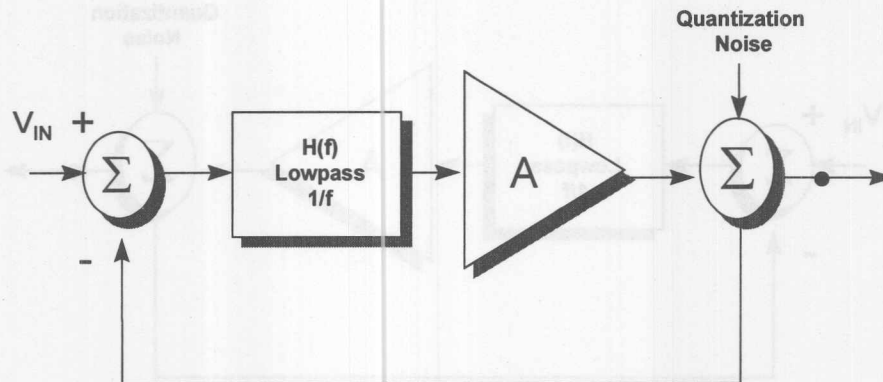
or

$$Y = x/(f+1) + qf/(f+1)$$

3-109



Noise Shaping (con't)

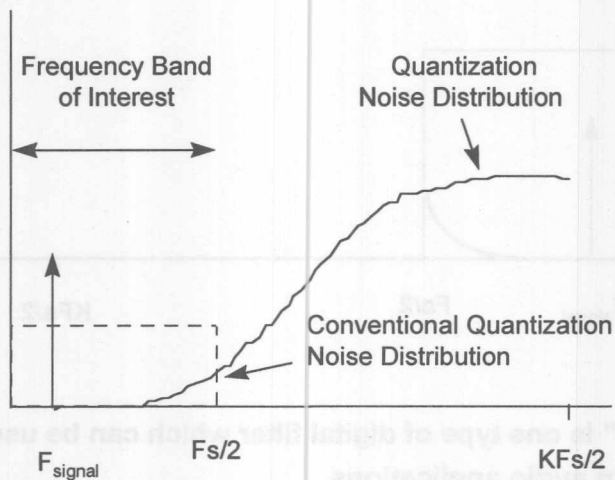


As f approaches 0, y approaches x (i.e. The input signal), and as f increases, y becomes dominated by q (quantization noise). So the signal concentrates itself in the low frequency region while the quantization noise is located in a higher frequency region. We call this phenomenon noise shaping. This is very different from a conventional converter where the quantization noise is evenly spread throughout the 0 to $f_s/2$ band.

3 - 110



Noise Shaping (con't)



The effect of noise shaping has been to place the undesired quantization noise/error in a high frequency band where it can easily be removed using a digital filter.

3 - 111



Digital Filtering

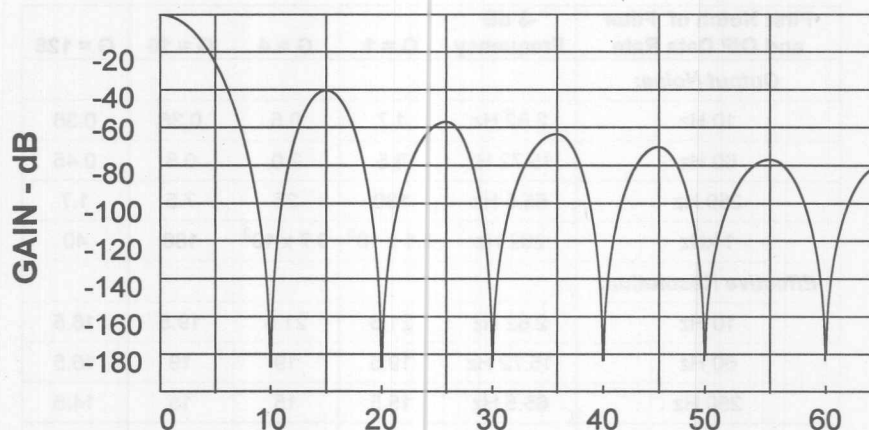


- A “Brickwall” is one type of digital filter which can be used. Brickwalls are popular in audio applications.
- Sometimes we use a different type of filter called a $(\sin x/x)^3$ or sync³ or sync-cubed filter.
- It is also easy to integrate the decimation circuitry into the digital filter

3 - 112



Digital Filter Response



The Filter has notches at multiples of the programmed output data rate. The default first notch frequency (and hence data rate) is typically 60Hz.

Depending on the specific Model, the first notch frequency can be set any where between about 2Hz and 1000Hz. As we increase the notch frequency, we will tend to see an increase in noise and subsequent loss in resolution.

3 - 113



Typical Output RMS Noise in μV and Effective Resolution in Bits

First Notch of Filter and O/P Data Rate	-3 dB Frequency	G = 1	G = 4	G = 16	G = 128
Output Noise:					
10 Hz	2.62 Hz	1.7	0.5	0.36	0.36
60 Hz	15.72 Hz	8.5	2.0	0.6	0.45
250 Hz	65.5 Hz	130	25	7.5	1.7
1 kHz	262 Hz	3.1×10^3	0.7×10^3	180	40
Effective Resolution:					
10 Hz	2.62 Hz	21.5	21.5	19.5	16.5
60 Hz	15.72 Hz	19.5	19	19	16.5
250 Hz	65.5 Hz	15.5	15	15	14.5
1 kHz	262 Hz	10.5	11	11	10

- Device (Semiconductor, Resistor) Noise Dominates at the Lower Frequencies (< 60 Hz notch)
- Quantization Noise Dominates at the Higher Frequencies

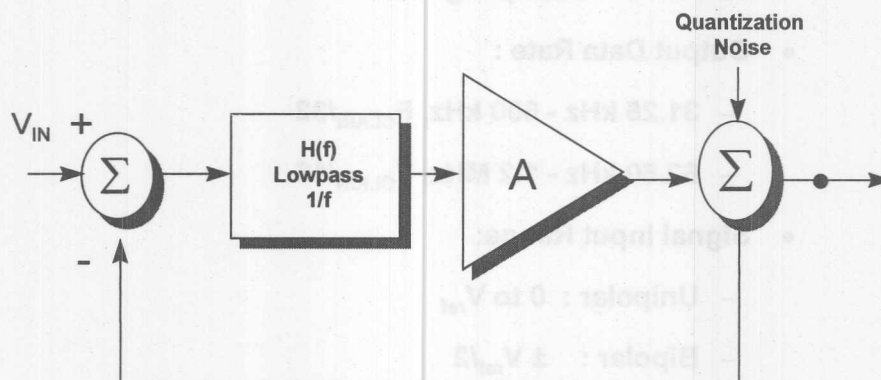
3 - 114



AD7723

1.2 MHz Sigma-Delta A/D Converter

The AD7723 provides true 16 bit performance for input bandwidths up to 460 kHz, at an output word rate up to 1.2 MHz. The sample rate, filter corner frequencies and output word rate are set by the crystal oscillator or external clock frequency



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AD7723 - Key Specs and Features

- Flexible 16 Bit Serial and Parallel Interface
- 1 MHz to 19.2 MHz Master Clock Frequency
- 32/16 X Oversampling Ratio
- Output Data Rate :
 - 31.25 kHz - 600 kHz, $F_{CLKIN}/32$
 - 62.50 kHz - 1.2 MHz, $F_{CLKIN}/16$
- Signal Input Range:
 - Unipolar : 0 to V_{ref}
 - Bipolar : $\pm V_{ref}/2$

3 - 116



AD7723 - Key Specs and Features (con't)

- **Dynamic Performance (Decimate by 32) :**
 - Signal to(Noise & Distortion) 87 dB, min
 - Total Harmonic Distortion : - 90 dB, max
- **Low Pass and Band Pass Digital Filter :**
 - Linear Phase
 - ± 0.001 dB Max Flatness, DC - 230 kHz
- **Internal 2.5 V Reference**
- **+ 5V Single Supply Operation**
 - 300 mW max, normal mode
 - 50 uW max, STANDBY mode

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Preliminary
Information

AD7705, AD7706 and AD7707* 16 Bit Sigma Delta A/D Converters

The AD7705, AD7706 and AD7707 are complete analog front ends for low level, low frequency measurement applications. They offer a choice of different input configurations...

- AD7705 • 2 Fully Differential Low Level Input Channels
- AD7706 • 3 Pseudo-Differential Low Level Input Channels
- AD7707 • 2 Pseudo-Differential Low Level Input Channels and 1 High Level Input Channel

3 - 118



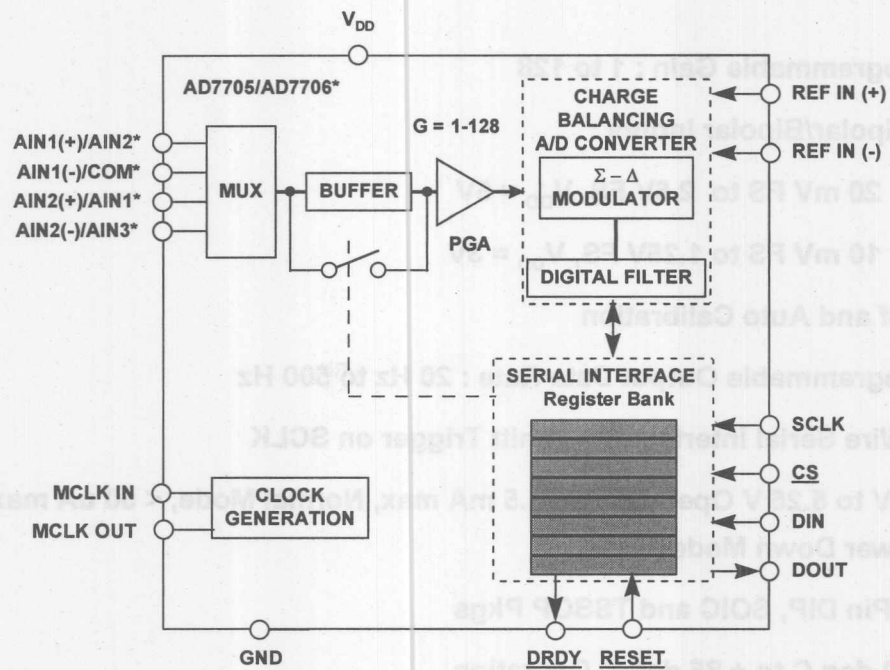
AD7705 - AD7707 : Key Specs and Features

- Programmable Gain : 1 to 128
- Unipolar/Bipolar Inputs :
 - 20 mV FS to 2.5V FS, $V_{DD} = 5V$
 - 10 mV FS to 1.25V FS, $V_{DD} = 3V$
- Self and Auto Calibration
- Programmable Output Data Rate : 20 Hz to 500 Hz
- 3 Wire Serial Interface : Schmitt Trigger on SCLK
- 2.7V to 5.25 V Operation : < 1.5 mA max, Normal Mode, < 50 uA max , Power Down Mode
- 16 Pin DIP, SOIC and TSSOP Pkgs
- - 40 deg C to + 85 deg C Operation

3-119



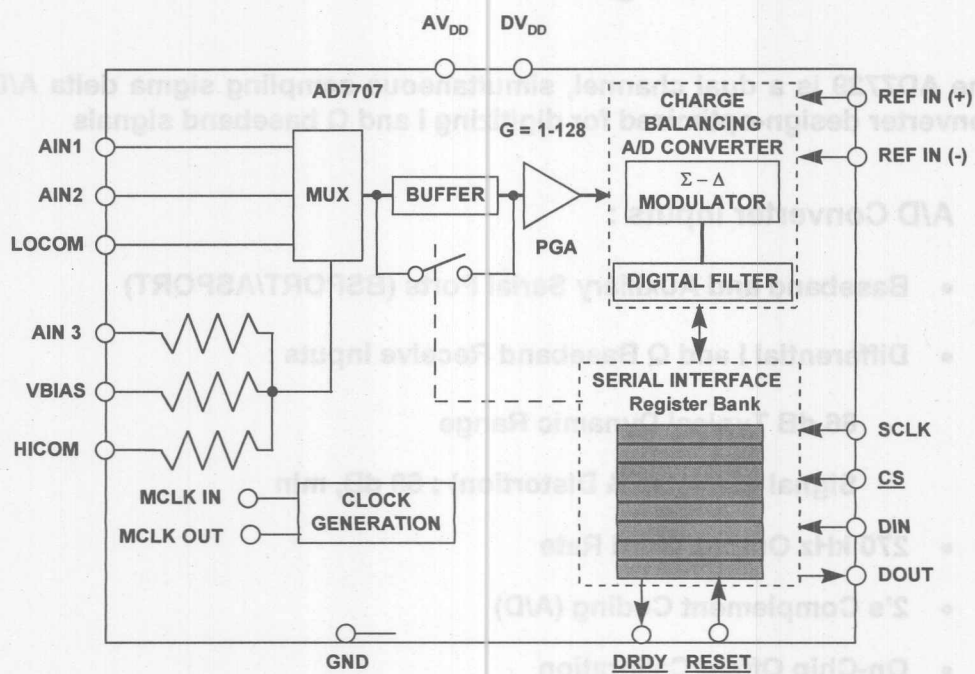
AD7705, AD7706 Block Diagram



3-120



AD7707 Block Diagram



3-121



AD7729

15 Bit, Sigma Delta A/D Converter

The AD7729 is a dual channel, simultaneous sampling sigma delta A/D converter design-optimized for digitizing I and Q baseband signals

A/D Converter Inputs :

- **Baseband and Auxiliary Serial Ports (BSPORT/ASPORT)**
- **Differential I and Q Baseband Receive Inputs :**
 - **66 dB Typical Dynamic Range**
 - **Signal to (Noise & Distortion) : 60 dB, min**
- **270 kHz Output Word Rate**
- **2's Complement Coding (A/D)**
- **On-Chip Offset Calibration**

3 - 122



AD7729 - Key Specs and Features (con't)

Auxiliary DAC Channel :

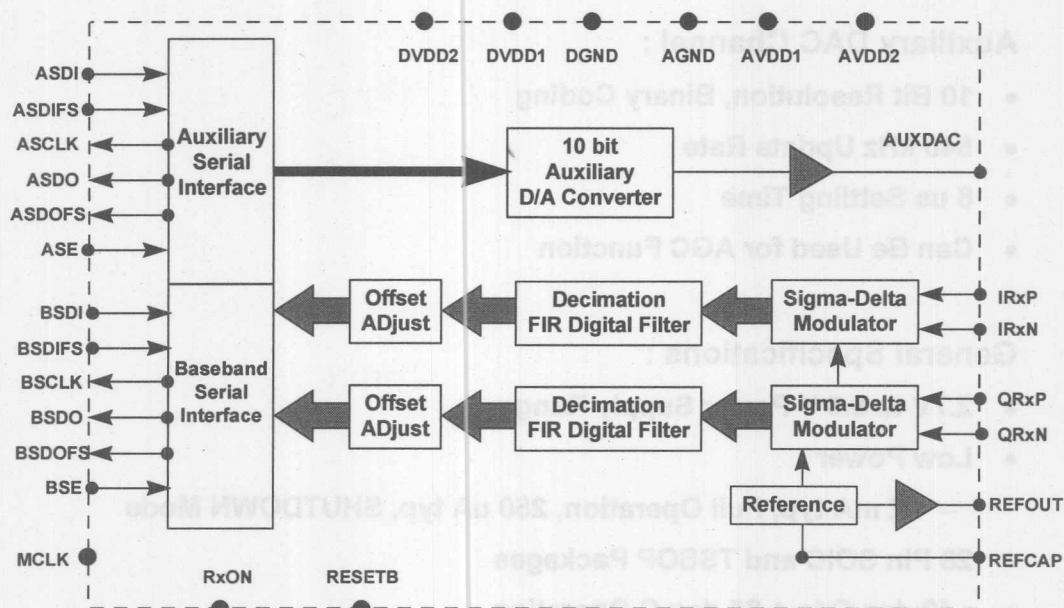
- 10 Bit Resolution, Binary Coding
- 540 kHz Update Rate
- 8 μ s Settling Time
- Can Be Used for AGC Function

General Specifications :

- 2.7V to 5.5 V Power Supply Range
- Low Power :
 - 32 mA typ, Full Operation, 250 μ A typ, SHUTDOWN Mode
- 28 Pin SOIC and TSSOP Packages
- - 40 deg C to + 85 deg C Operation



AD7729 - Simplified Diagram



3 - 124



Special Function Products

Energy Metering A/D Converters



*** Preliminary
Information**

AD7751*

Energy Metering IC with On-Chip Fault Detection

- High Accuracy, Supports 50/60 Hz IEC 521/1036
- Less Than 0.3% Error Over 500:1 Dynamic Range
- Average Real Power at F1 and F2 Low Frequency Outputs :
 - Can Be Used As Direct Drive for Electromechanical Counters or 2 Phase Stepper Motors
- Instantaneous Real Power at High Frequency CF Output
- Continuous Monitoring of the Phase and Neutral Currents
Allows Fault Detection in 2-Wire Distribution Systems

3 - 126



AD7751 (con't)

- **REVP and FAULT Logic Outputs Indicate Mis-Wiring or Fault Condition**
- **Current Input Channel Has PGA to Allow Use of Small Values of Shunt and Burden Resistance**
- **User-Selectable Timed Reset of AD7751 on Power up/Power Down**
- **Single +5V Operation, 15 mW Typical Dissipation**
- **24 Pin DIP and SSOP Packages**

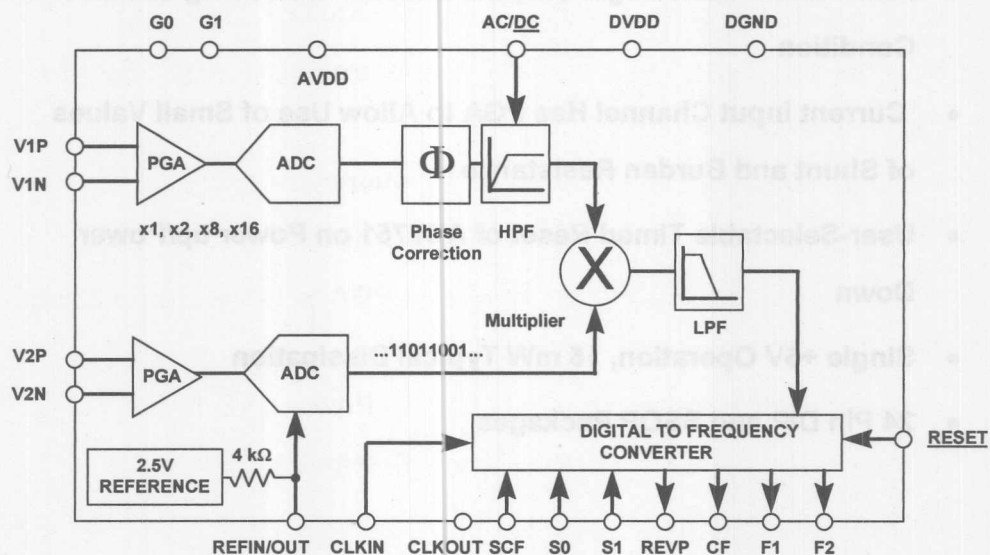
3 - 127



* Preliminary
Information

AD7755* Energy Metering IC w/Pulse Output

The AD7755 is a high accuracy electrical energy measurement IC intended for use with 2-wire distribution systems. The part specifications surpass the accuracy requirements as quoted in the IEC-1036 Standard



3 - 128



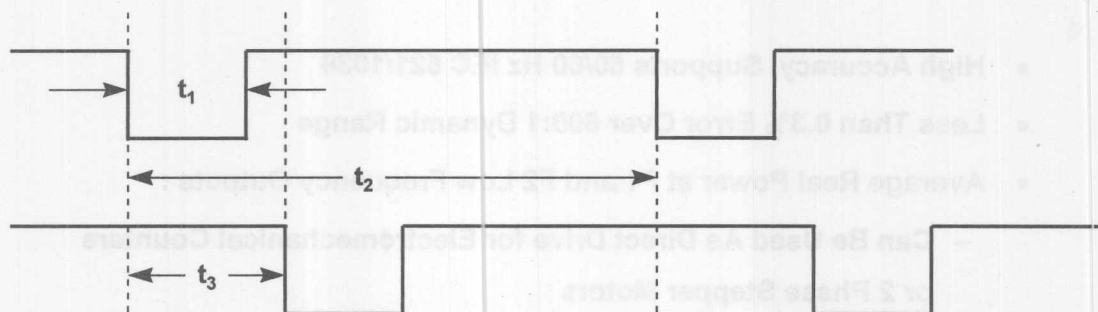
AD7755 - Key Specs and Features

- **High Accuracy, Supports 50/60 Hz IEC 521/1036**
- **Less Than 0.3% Error Over 500:1 Dynamic Range**
- **Average Real Power at F1 and F2 Low Frequency Outputs :**
 - **Can Be Used As Direct Drive for Electromechanical Counters or 2 Phase Stepper Motors**
- **Instantaneous Real Power at High Frequency CF Output**
- **REVP Logic Output Indicates Negative Power or Mis-Wiring**
- **Current Input Channel (V1P, V1N) Has PGA to Allow Use of Small Values of Shunt and Burden Resistance**
- **User-Selectable Timed Reset of AD7755 Power up/Down**
- **Single +5V Operation, 15 mW Typical Dissipation**
- **24 Pin DIP and SSOP Packages**

3 - 129



Frequency Outputs, F1 & F2



S1	S0	Max Frequency for DC Inputs (Hz)	Max Frequency for AC Inputs (Hz)
0	0	0.17	0.0854
0	1	0.34	0.17
1	0	0.68	0.34
1	1	1.36	0.68

3 - 130



*** Preliminary
Information**

AD7756* Energy Metering IC with Serial Port Interface

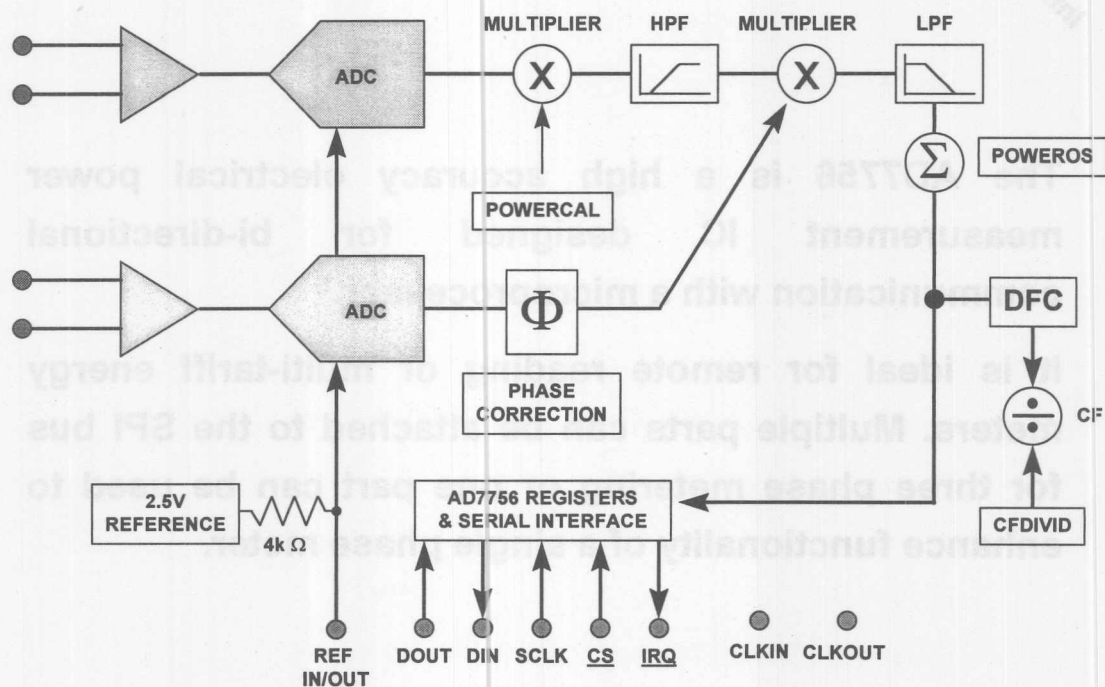
The AD7756 is a high accuracy electrical power measurement IC designed for bi-directional communication with a microprocessor.

It is ideal for remote reading or multi-tariff energy meters. Multiple parts can be attached to the SPI bus for three phase metering or one part can be used to enhance functionality of a single phase meter.

3-131



AD7756 - Simplified Diagram



3 - 132



AD7756 - Key Specs and Features

- **High Accuracy, Supports 50/60 Hz IEC 521/1036**
- **Less Than 0.2% Error Over a Dynamic Range of 500 :1**
- **SPI-Compatible Serial Interface**
- **Internal 2.5V Reference With External Overdrive Capability**
- **External Reset Allows for Low Cost Power Supply**
- **Maskable Interrupt [Open Drain]**
- **Zero Crossing Pin [Open Drain]**
- **Low Voltage Detection [Active Low Pin]**
- **High Frequency Output Pin for Calibration and Test**
- **Single +5V Supply, 15 mW typical**
- **20 Pin PDIP and SSOP Packages**

3 - 133



AD7756 - Read/Write Register Contents

- **Phase, Gain, Offset, and Input Calibration Coefficients**
- **Instantaneous Real Power (16 Bits)**
- **Active Energy (40 Bits)**
- **Reverse Polarity Flag**
- **Line Voltage Monitoring**
- **Program Register for Output Frequency**
- **Current or Voltage Waveform Samples Captured at 28KSPS Word Data Rate**
- **Low Power Mode**
- **Self Diagnostic Mode**

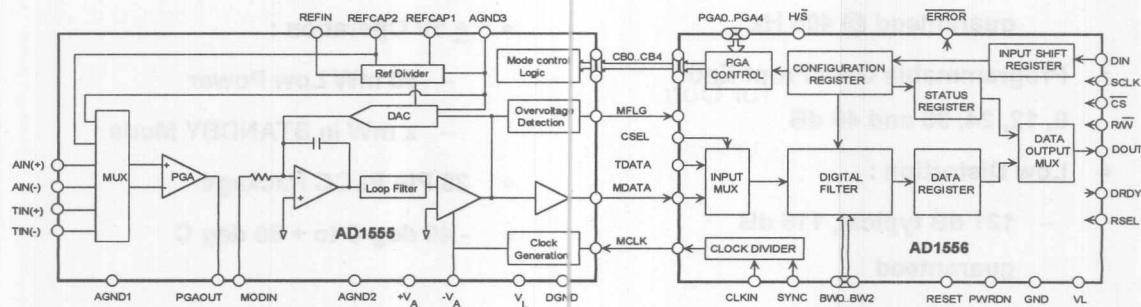
3 - 134



*** Preliminary
Information**

AD1555*, AD1556* 24 Bit ADC Chip-set for Seismic Applications

The AD1555 and AD1556 is a high resolution data acquisition chipset developed for seismic and other applications requiring extremely high resolution and THD performance.



3 - 135



AD1555 Key Specs and Features...

- **4th Order Sigma-Delta Modulator**
- **Large Dynamic Range :**
 - 121 dB typical, 118 dB guaranteed @ 405 Hz
- **Programmable Gain Front End :**
 - 0, 12, 24, 36 and 48 dB
- **Low Distortion :**
 - 121 dB typical, 116 dB guaranteed
- **Sampling Rate : 256 ksp/s**
- **High Jitter Tolerance**
- **No Anti-Alias Filter Required**
- **$\pm 2.25\text{V}$ Input Range**
- **$\pm 5\text{V}$ Operation :**
 - 80 mW Low Power
 - x mW in STANDBY Mode
- **28 Pin PLCC Package**
- **- 40 deg C to + 85 deg C**

3 - 136



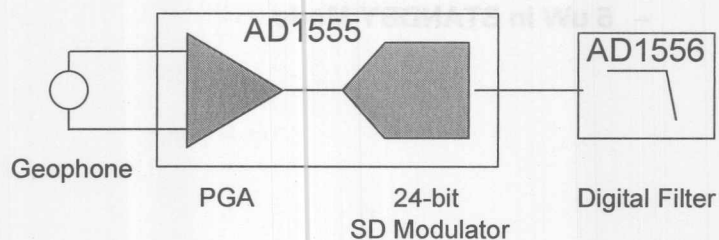
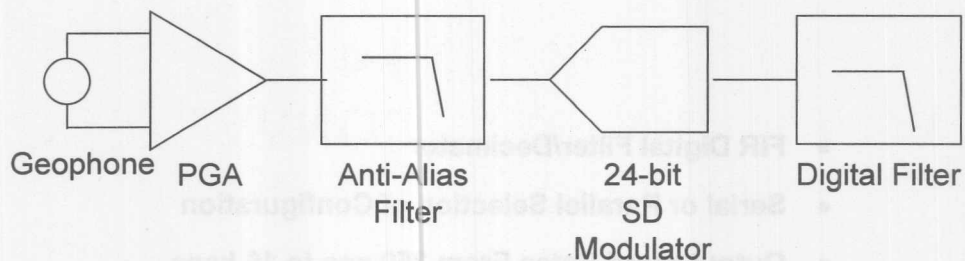
AD1556 Key Specs and Features...

- **FIR Digital Filter/Decimator**
- **Serial or Parallel Selection of Configuration**
- **Output Word Rates From 250 sps to 16 ksps**
- **+ 5V Operation :**
 - **20 mW Normal Mode**
 - **5 μ W in STANDBY Mode**

3 - 137



Current Seismic Solution vs AD1555/AD1556



3 - 138



SECTION 4

DIGITAL- ANALOG CONVERTERS

**High Speed
Interpolating
High Resolution
Direct Digital Synthesis
Single Supply, Low Power**



DIGITAL-ANALOG CONVERTERS SECTION 4

Single Supply, Low Power
Direct Digital Synthesis
High Resolution
Interpolating
High Speed

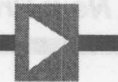


High Speed D/A Converters

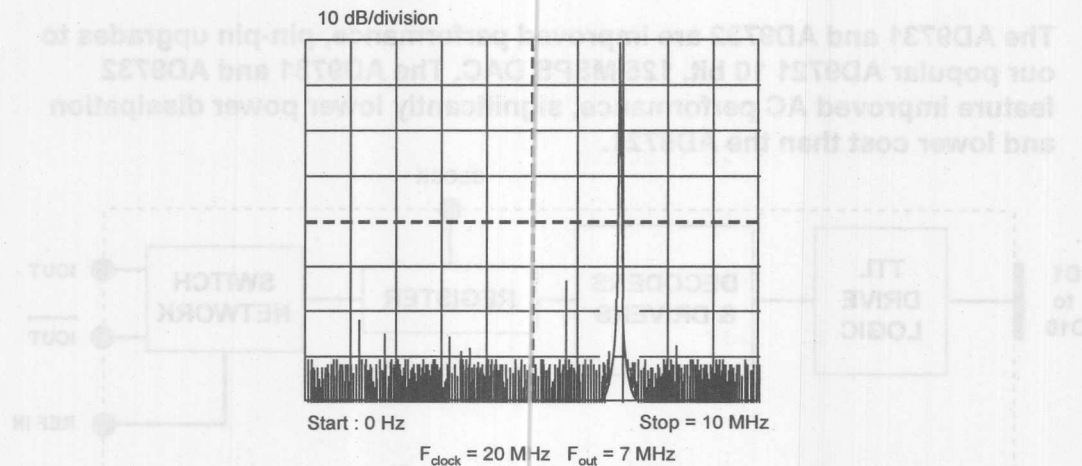


Which Specs are Important for High Speed DACs?

- **High Speed DACs Traditionally Characterized by, -**
 - **DNL, INL, Monotonicity**
 - **Settling Time**
 - **Glitch Impulse**
- **Specs not Sufficient for Communications and Video Imaging Applications**



Important High Speed DAC Specs (con't)



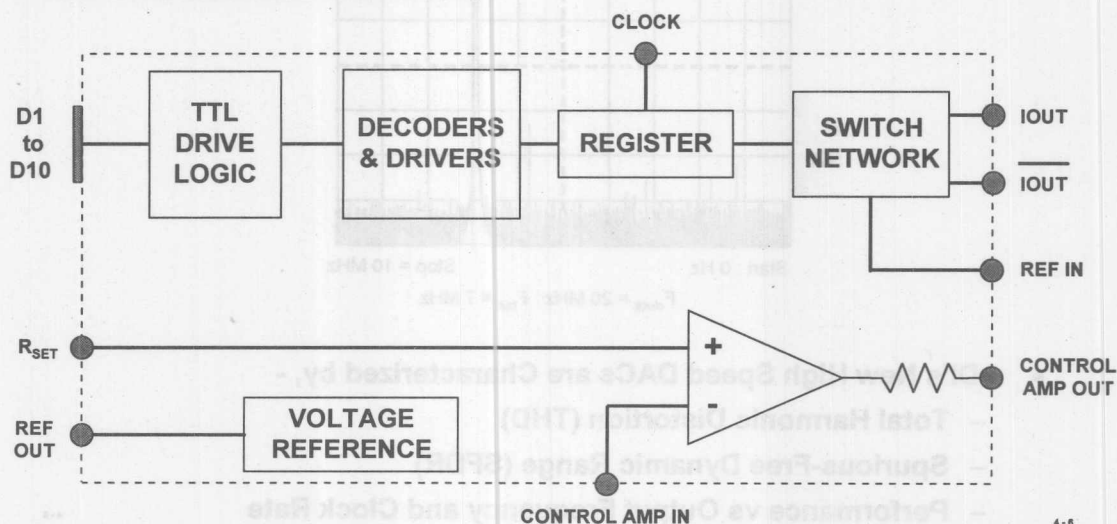
- ADI's New High Speed DACs are Characterized by, -
 - Total Harmonic Distortion (THD)
 - Spurious-Free Dynamic Range (SFDR)
 - Performance vs Output Frequency and Clock Rate

4-5



AD9731, AD9732 10-Bit, 170/200 MSPS D/A Converters

The AD9731 and AD9732 are improved performance, pin-pin upgrades to our popular AD9721 10 bit, 125 MSPS DAC. The AD9731 and AD9732 feature improved AC performance, significantly lower power dissipation and lower cost than the AD9721.



4-6

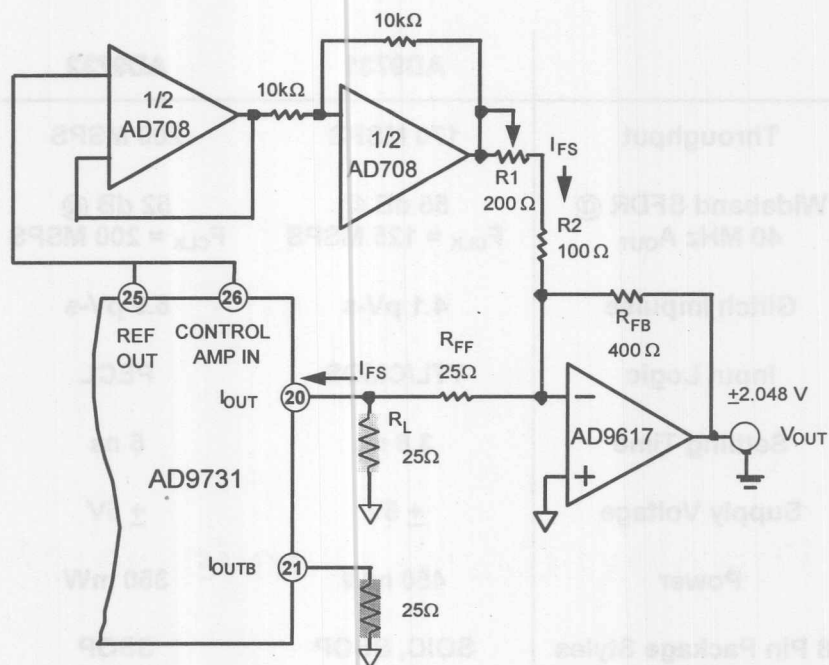
**AD9731 and AD9732 - Key Specs and Features**

	AD9731	AD9732
Throughput	170 MSPS	200 MSPS
Wideband SFDR @ 40 MHz A_{OUT}	55 dB @ F_{CLK} = 125 MSPS	52 dB @ F_{CLK} = 200 MSPS
Glitch Impulse	4.1 pV-s	5.9 pV-s
Input Logic	TTL/CMOS	PECL
Settling Time	3.8 ns	5 ns
Supply Voltage	± 5V	± 5V
Power	450 mW	350 mW
28 Pin Package Styles	SOIC, SSOP	SSOP

4-7



I-V Conversion





**10-14 Bit
High Speed,
TxDAC[™] (“Transmit DAC”)
Family**

The Next Generation is Here!



AD97XX TxDAC™ (“Transmit DAC”) Family

Analog Devices' next generation of 10-14 bit, 125 - 200 MSPS “Transmit DACs” are design-optimized and characterized for communications and video imaging applications, and feature...

- *Superior Dynamic Performance*
- *Single 3V-5V or 5V Operation*
- *CMOS, Low Power : < 75 mW with 3V Supply*
- *Family Pin Compatibility*
- *Low Cost*
- *Small SOIC, TSSOP Packages*

4 - 10



The "Transmit DAC" Family at a Glance...

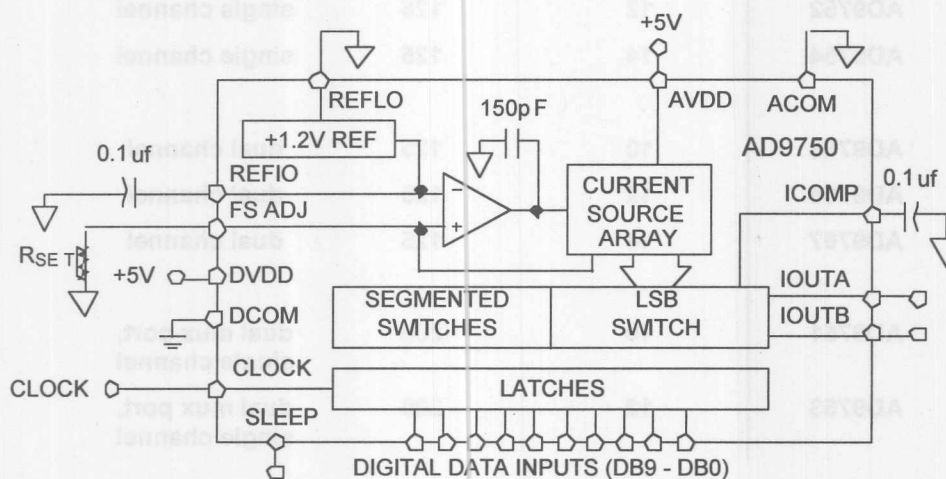
	Bits	Update Rate, MSPS	Comment
AD9750	10	125	single channel
AD9752	12	125	single channel
AD9754	14	125	single channel
AD9763	10	125	dual channel
AD9765	12	125	dual channel
AD9767	14	125	dual channel
AD9751	10	200	dual mux port, single channel
AD9753	12	200	dual mux port, single channel

4 - 11



AD9750, AD9752 and AD9754 10/12/14 Bit, 125 MSPS, TxDAC™ Family

The AD975X Family represents Analog Devices' 2nd generation TxDAC™ series of high performance, low power CMOS D/A Converters



4-12



AD975X Family - Key Specs and Features

- **High Speed Settling : 35 ns to 0.1 %**
- **Low Glitch Impulse : 5 pV-sec**
- **Excellent SFDR to Nyquist : > 80 dBc¹**
- **Total Harmonic Distortion: > - 80 dBc¹**
- **Differential Current Outputs : 2 mA to 20 mA**
- **Single +2.7V to + 5.5V, Low Power Operation:**
 - **220 mW Normal Mode, 40 mW Power Down Mode**
- **On-Chip 1.2 V Reference**
- **Pin Compatibility within the TxDAC™ Family**
- **28 Pin SOIC, TSSOP Packages**

1 : F_{CLOCK} = 25 MSPS, and F_{OUT} = 1 MHz

4 - 13



Preliminary
Information

AD9763*, AD9765* and AD9767* 10/12/14 Bit Dual 125 MSPS TxDAC™ Converters

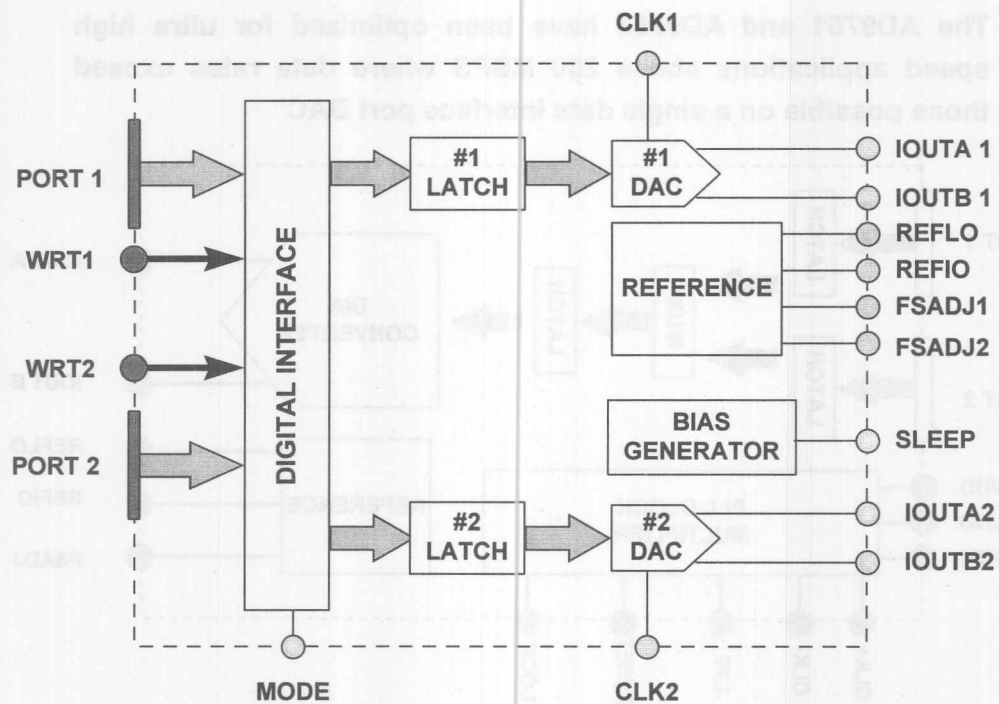
Same Excellent Performance as the TxDAC Family, Plus...

- Excellent Gain and Offset Matching :
 - Gain : $< 0.5\%$
 - Offset : $< 0.025\%$
- Dual Port or Interleaved Data
- Single +2.7V to + 5.5V, Low Power Operation:
 - < 400 mW Normal Mode
 - < 40 mW SLEEP Mode
- 48 Pin LQFP Package
- - 40 deg C to + 85 deg C

4-14



AD9763/65/67 - Block Diagram



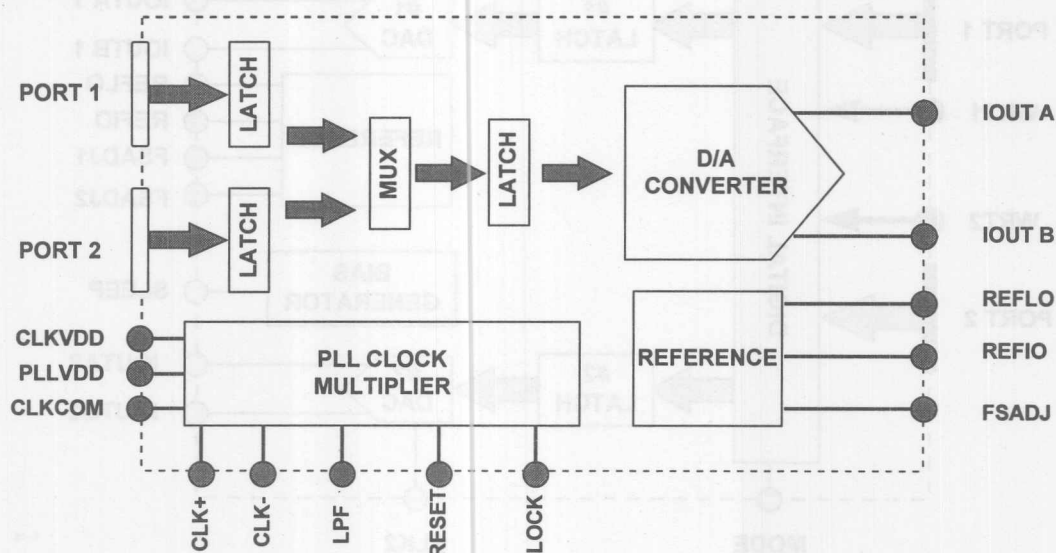
4-15



Preliminary
Information

AD9751*, AD9753* 10/12 Bit, 200 MSPS TxDAC™ D/A Converters

The AD9751 and AD9753 have been optimized for ultra high speed applications above 200 MSPS where data rates exceed those possible on a single data interface port DAC





AD9751, AD9753 - Key Specs and Features

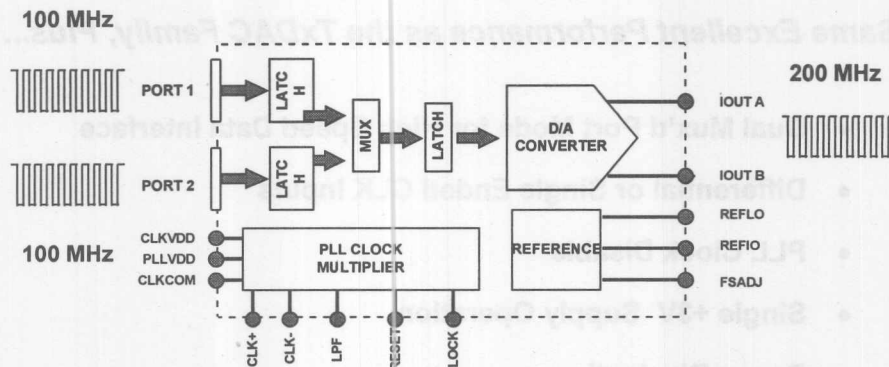
Same Excellent Performance as the TxDAC Family, Plus...

- **Dual Mux'd Port Mode for High Speed Data Interface**
- **Differential or Single Ended CLK Inputs**
- **PLL Clock Disable**
- **Single +3V Supply Operation**
- **Power Dissipation :**
 - **< 300 mW in Normal Mode**
 - **< 25 mW in Power Down Mode**
- **- 40 deg C to + 85 deg C**
- **48 Pin LQFP Package**

4-17



AD9751, AD9753 - Dual Muxed Port



- Dual Port Data Is Time-Multiplexed to the Internal High Speed DAC via 2 Ranks of Latches.
- The Internal PLL Drives the Latches at 2X the Speed of the External CLK
- Data From Both Ports Is Interleaved to the DAC
- Output Data Rate Is 2X Either Input Rate

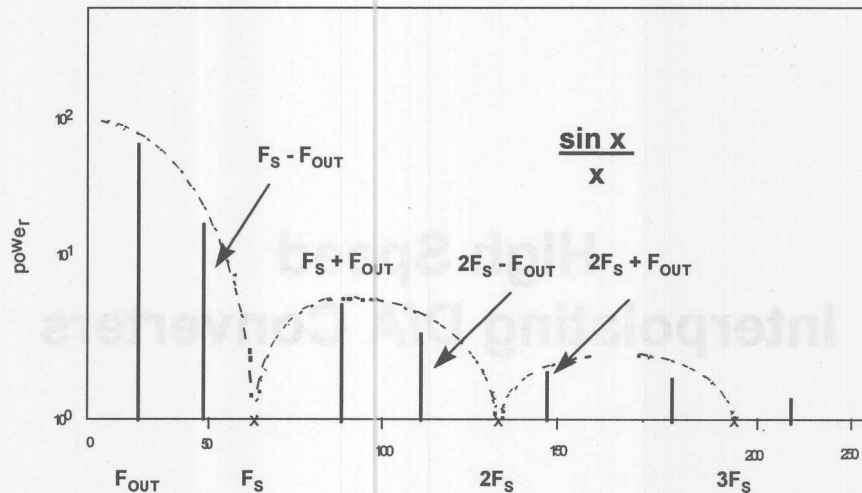
4-18



High Speed Interpolating D/A Converters



DAC Images



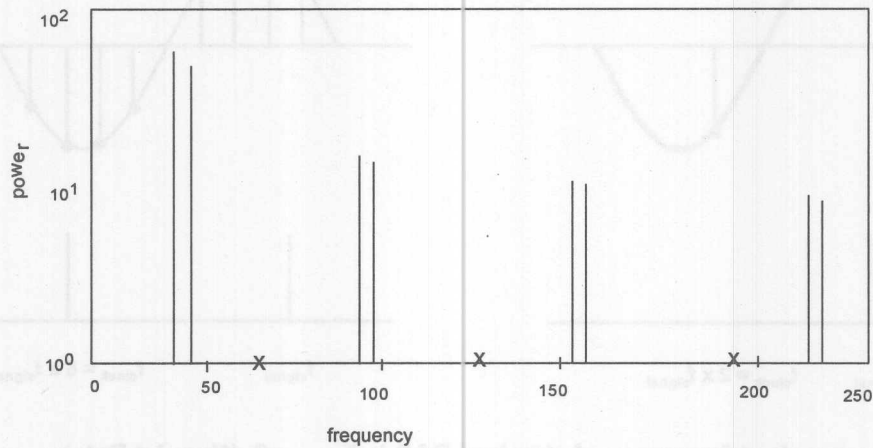
The output of a reconstruction DAC contains “images” (similar to “aliasing” in an ADC...remember Nyquist Theory?) that are multiples of the clock or sampling frequency \pm the DAC output, F_{OUT} .

In the above example, $F_{OUT} = 0.29 \times F_S$

4 - 20



DAC Images (con't)

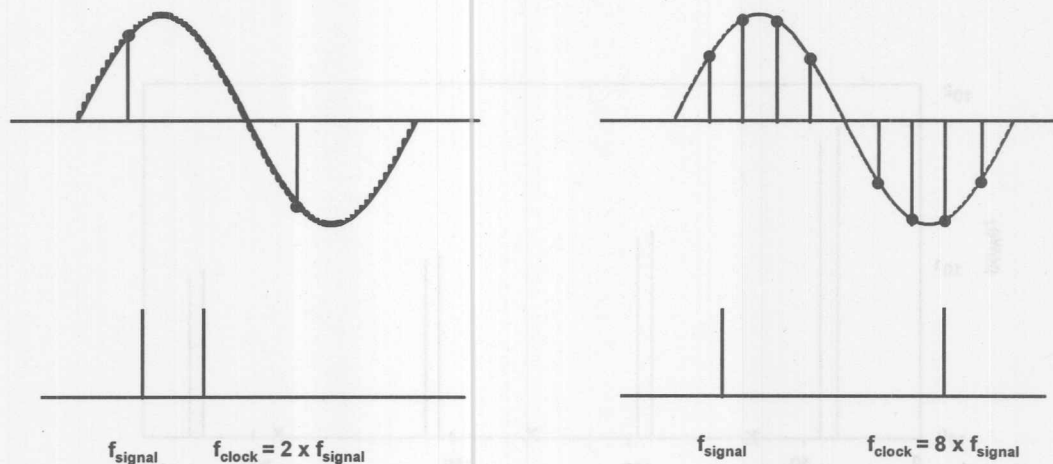


As the DAC output (F_{OUT}) approaches Nyquist frequency (in the above example $F_{OUT} = 0.45 \times F_S$) the images become closer together, making it extremely difficult to filter the image from the signal.

4-21



Interpolation

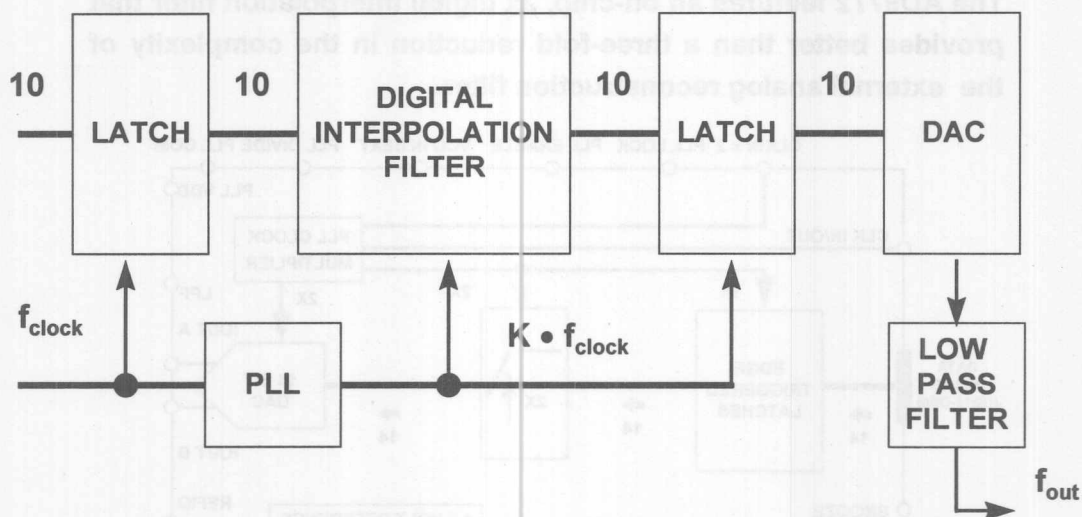


- Maximum output frequency of standard DAC is $F_{\text{clock}} \div 2$ (Nyquist Rate)
- In an Interpolating D/A Converter, Digital Interpolation Filters and a PLL Clock Multiplier are used to multiply the input data rate to the DAC by a factor of X times the clock rate...this produces an image at x times F_{signal} , smoothing the sine function and simplifying the filter requirements

4 - 22



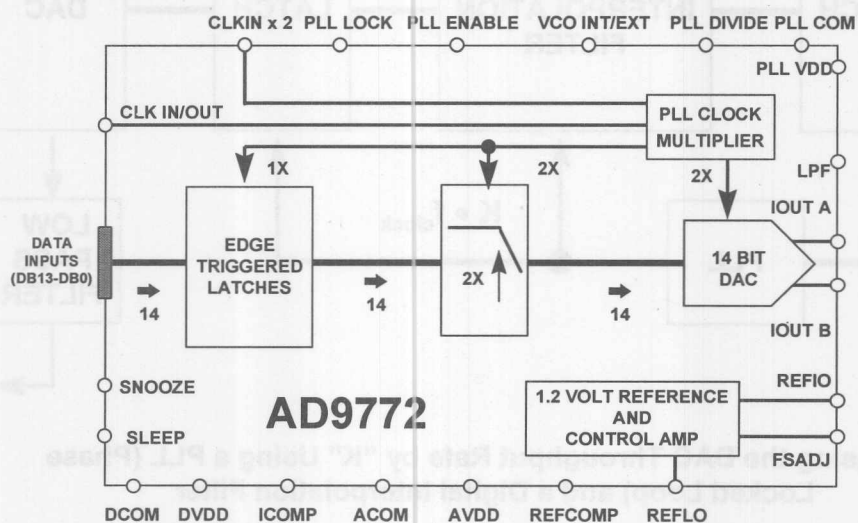
Interpolating DAC



Increasing the DAC Throughput Rate by “K” Using a PLL (Phase Locked Loop) and a Digital Interpolation Filter

4 - 23

The AD9772 features an on-chip, 2x digital interpolation filter that provides better than a three-fold reduction in the complexity of the external analog reconstruction filter.



4.34



AD9772 - Key Specs and Features

- **125 MSPS Maximum Input Clock Rate**
- **250 MSPS Maximum Output Update Rate**
- **52 MHz Reconstruction Bandwidth**
- **Output Settling Time : 35 ns to 0.025%**
- **Glitch Impulse : 5 pV-s**
- **2 mA to 20 mA Output Current Range**
- **Single +2.7V to +3.3V Operation**
- **- 40 deg C to+ 85 deg C Operation**
- **48 Pin LQFP Package**

4 - 25



AD9772 - Key Specs and Features

- 128 MSPS Maximum Input Clock Rate
- 280 MSPS Maximum Output Update Rate
- 82 MHz Reconstruction Bandwidth
- Output Settling Time : 38 ns to 0.025%
- Glitch Impulse : 8 pV-s
- 2 mA to 20 mA Output Current Range
- Single +2.7V to +3.3V Operation
- -48 deg C to +85 deg C Operation
- 68 Pin LQFP Package

4 - 26

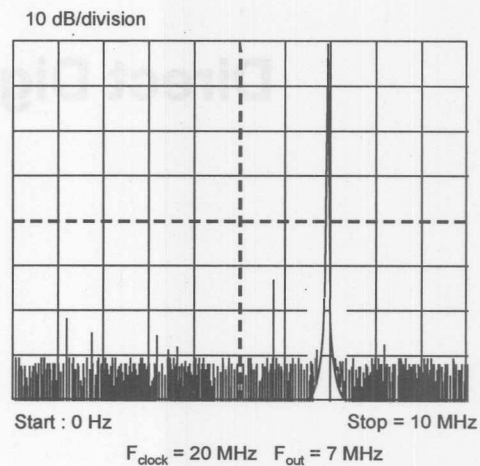
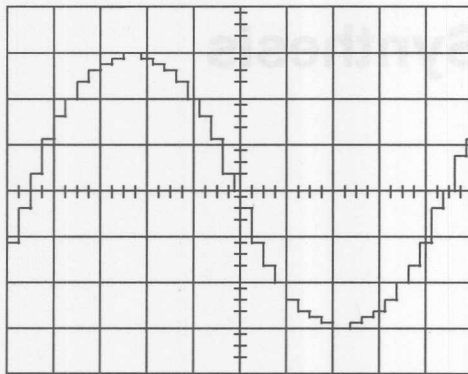


Direct Digital Synthesis



What is Direct Digital Synthesis?

Direct Digital Synthesis (DDS) is a technique which allows one to generate high frequency, spectrally pure sinewaves of varying frequencies.



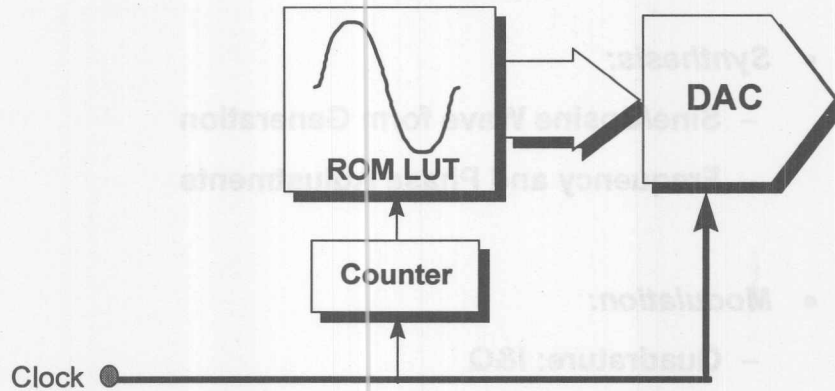


Where is Direct Digital Synthesis Used?

- **Synthesis:**
 - Sine/Cosine Wave form Generation
 - Frequency and Phase Adjustments
- **Modulation:**
 - Quadrature: I&Q
 - Frequency
 - Phase
 - Amplitude



Basic Waveform Generator

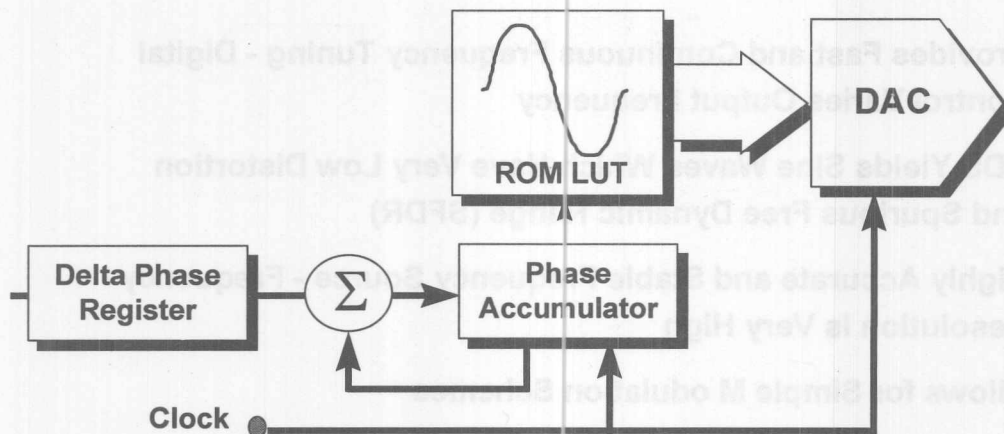


- On each cycle of the clock, the address pointer moves by one position in the Look Up Table (LUT) and the DAC is updated, which yields a sine wave of constant frequency.
- But how can we vary the output frequency without having to vary the clock speed?

4 - 30



Phase Accumulator



The frequency of the sinewave depends on the step size of the phase accumulator, so we actually write a phase increment to the device (not a frequency)

4 - 31



Advantages of Direct Digital Synthesis

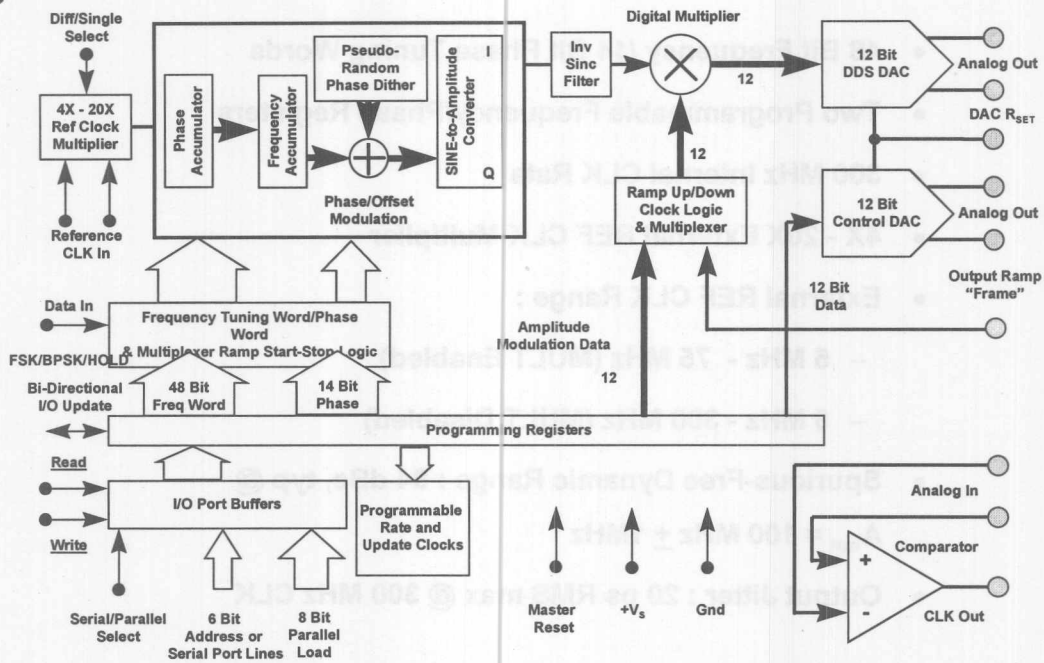
- **Provides Fast and Continuous Frequency Tuning - Digital Control Varies Output Frequency**
- **DDS Yields Sine Waves Which Have Very Low Distortion and Spurious Free Dynamic Range (SFDR)**
- **Highly Accurate and Stable Frequency Source - Frequency Resolution Is Very High**
- **Allows for Simple Modulation Schemes**
- **Can Provide Quadrature Frequency Outputs**

4 - 32



Preliminary
Information

AD9852* 300 MHz Direct Digital Synthesizer



4 - 33



AD9852 - Key Specs and Features

- 48 Bit Frequency /14 Bit Phase Tuning Words
- Two Programmable Frequency/Phase Registers
- 300 MHz Internal CLK Rate
- 4X - 20X External REF CLK Multiplier
- External REF CLK Range :
 - 5 MHz - 75 MHz (MULT Enabled)
 - 5 MHz - 300 MHz (MULT Disabled)
- Spurious-Free Dynamic Range : 84 dBc, typ @
 $A_{out} = 100 \text{ MHz} \pm 1\text{MHz}$
- Output Jitter : 20 ps RMS max @ 300 MHz CLK

4-34



AD9852 - Key Specs and Features (con't)

- Amplitude Ramping/Modulation Functions
- Single Pin FSK and PSK Data Interface
- FM Chirp Function
- High Speed Comparator Output : > 200 MHz
- Single +3.3V Supply Operation : 800 mW Normal Mode, 10 mW Power Down Mode
- 64 Pin LQFP Package
- - 40 deg C to + 85 deg C Operation

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AD9852 - Synthesizer Descriptions

- **Pseudo-Random Sequence Generator** – User-selectable function embedded in the DDS to generate pseudo-random phase offset “dither” in the 48-bit phase word from the phase accumulator, for reducing DDS spurious emissions (“spurs”). Dithering in the AD9852 occurs at the system clock rate, 300 MHz maximum.
- **Output Ramp Control** – Allows controlled output amplitude ramping or “framing” of the DDS DAC output. Ramping is controlled via a 12-bit digital multiplier prior to the DDS DAC. Output ramping reduces spurious emissions due to abrupt changes in the DAC output envelope.
- **DDS DAC** – this is the 300 MSPS cosine wave output of the DDS. Its maximum output amplitude is set by the DAC R_{SET} resistor. Full-scale maximum output of 20 mA.
- **Control DAC** – May be used to provide DC control levels to external circuitry, user-defined AC/DC signals, or to enable pulse-width modulation (PWM), or duty cycle control, of the on-board comparator 100 MHz update rate.

4 - 36



AD9852 - Synthesizer Descriptions (con't)

- **REFCLK Multiplier** – The internal system clock is generated by programming an integer multiple of the external reference clock between 4X - 20X. This function can be bypassed to allow direct clocking of the AD9852 from the external clock source.
- **48-bit Phase Accumulator** – programming this register in conjunction with I/O update will cause a single frequency to be output from the DDS with a resolution of 1 micro-Hertz. This accumulator operates at the DDS system clock (300 MHz maximum). FM modulation may be implemented here.
- **48-bit Frequency Accumulator** – programming this register in conjunction with the Ramp Rate Clock and I/O update allows automatic frequency incrementing or decrementing to occur at a rate set by the 20-bit Ramp Rate Clock. This accumulator allows automatic, user-defined frequency sweeping, ramping or CHIRPing.
- **FSK/PSK Data in** – this single pin data input selects one of two 48-bit frequency or 14-bit phase registers according to the logic level of the FSK or PSK data and user-defined control register programming.

4 - 37



AD9852 - Synthesizer Descriptions (con't)

- **Phase Offset/Modulation Register** – Sets the output phase of the DDS with .022 degree resolution. Can be updated at a 100 MHz rate through the I/O Buffers. PM and other phase modulation modes (such as QPSK) can be implemented using this register.
- **FSK Frequency “ramping”** – Allows shaping of the frequency transition from a “mark” to “space” frequency for bandwidth containment. User programs the two FSK frequencies, the resolution of frequency steps between the two FSK frequencies and finally, the 20-bit ramp rate clock.
- **FM CHIRP** – The user programs a start and stop frequency, the frequency step resolution and rate of change (ramp rate clock). CHIRP stops when the stop frequency is achieved, a HOLD command is issued, or when a value of 0 is loaded as a frequency step resolution. Furthermore, during a CHIRP sequence, the rate of change can be changed to achieve “piece-wise” shaping of the CHIRP sequence if a non-linear response is desired. GMSK and GFSK can be implemented in this mode.

4 - 38



**Preliminary
Information**

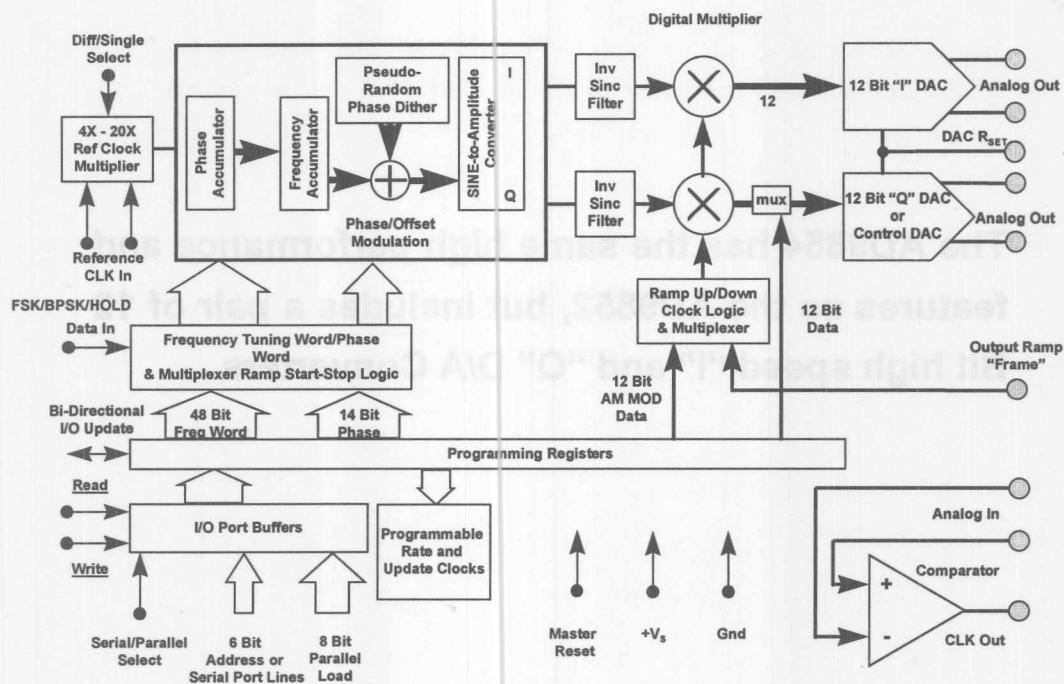
AD9854* **300 MHz Quadrature Direct Digital Synthesizer**

The AD9854 has the same high performance and features as the AD9852, but includes a pair of 12 Bit high speed “I” and “Q” D/A Converters

4-39



AD9854 - Block Diagram

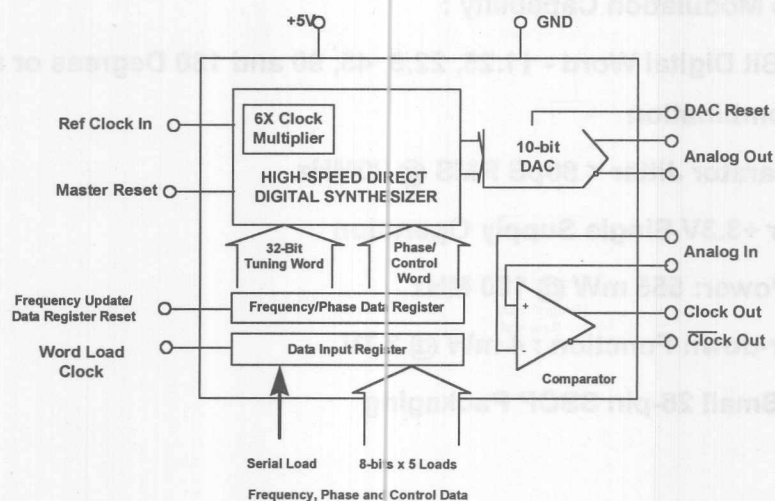


4 - 40



AD9851 180 MHz Direct Digital Synthesizer

The AD9851 is a highly integrated device that uses advanced DDS technology, coupled with an internal high speed D/A converter and comparator, to form a digitally-controlled frequency synthesizer and clock generator



4 - 41



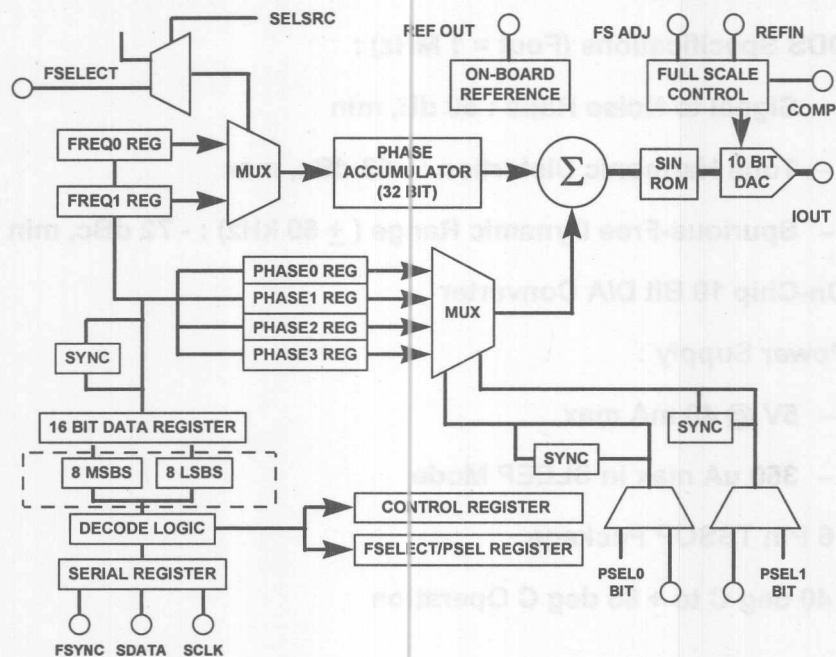
AD9851 - Key Specs and Features

- **Spurious-Free Dynamic Range >43 dB@ 70 MHz Aout**
- **32-bit Frequency Tuning Word**
- **Asynchronous Parallel or Serial Loading Format**
- **Phase Modulation Capability :**
 - **5 Bit Digital Word - 11.25, 22.5, 45, 90 and 180 Degrees or any Combination**
- **Comparator Jitter < 80pS RMS @ 20MHz**
- **+5V or +3.3V Single Supply Operation**
- **Low Power: 555 mW @ 180 MHz**
- **Power-down Function : 4 mW @ 2.7V**
- **Ultra-Small 28-pin SSOP Packaging**

4-42



AD9835 50 MHz Direct Digital Synthesizer



4-43



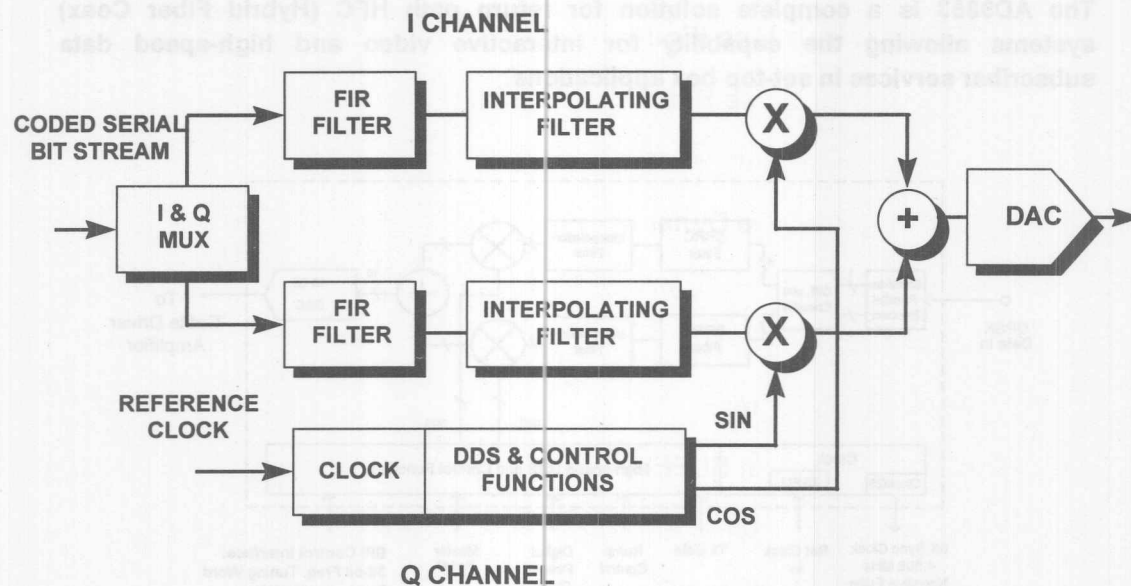
AD9835 - Key Specs and Features

- Serial Loading
- DDS Specifications ($F_{out} = 1 \text{ MHz}$) :
 - Signal to Noise Ratio : 50 dB, min
 - Total Harmonic Distortion : - 53 dBc, max
 - Spurious-Free Dynamic Range ($\pm 50 \text{ kHz}$) : - 72 dBc, min
- On-Chip 10 Bit D/A Converter
- Power Supply :
 - 5V @ 40 mA max
 - 350 uA max in SLEEP Mode
- 16 Pin TSSOP Package
- - 40 deg C to + 85 deg C Operation

4-44



A Typical I and Q Modulator

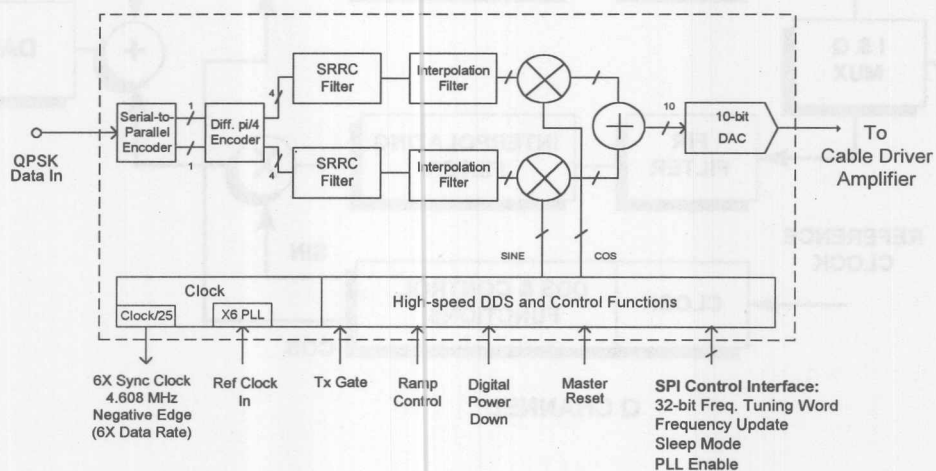


4 - 45



AD9853 Digital QPSK/16-QAM Modulator

The AD9853 is a complete solution for return path HFC (Hybrid Fiber Coax) systems allowing the capability for interactive video and high-speed data subscriber services in set-top box applications.



4 - 46



AD9853 - Key Specs and Features

- **Return Channel Tx Functions : 5 MHz - 42 MHz, 5 MHz - 65 MHz**
- **Frequency Tuning Word: 32-bit Serial Load**
- **165 MHz Internal Reference Clock Rate**
- **6X Internal Reference Clock Multiplier**
- **Modulation Formats : FSK, QPSK, DQPSK, 16-QAM, D16-QAM**
- **Controlled Burst Mode Function**
- **Programmable Pulse-Shaping FIR and Interpolating Filters**
- **Programmable Randomizer/Preamble Function**

4 - 47



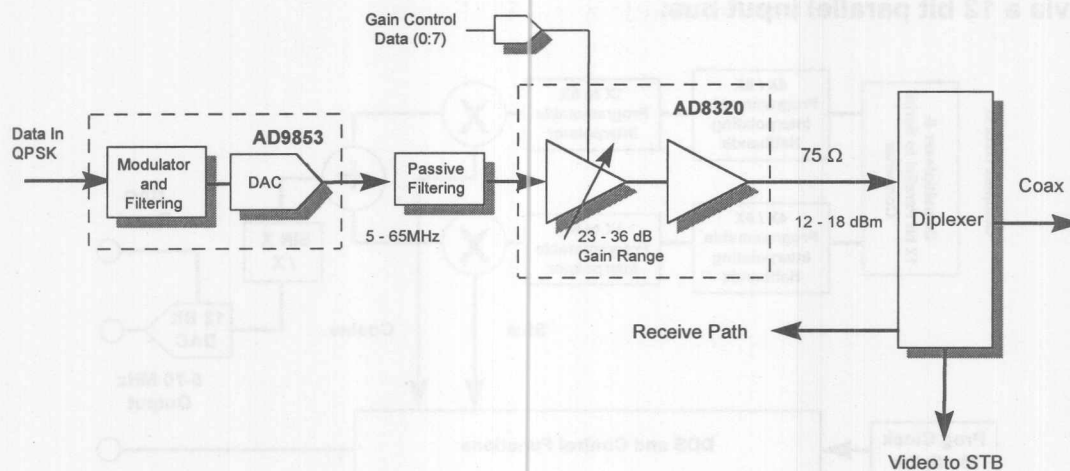
AD9853 - Key Specs and Features (con't)

- **Integrated Reed-Solomon FEC Function**
- **Internal Sin X/X Compensation**
- **Wideband SFDR (Single Tone) : 68 dBc @ 1 MHz, 50 dBc @ 42 MHz**
- **+ 3.3 V to + 5.0 V Single Supply Operation**
- **Low Power : 750 mW @ Full Clock Speed @ + 3.3V Supply**
- **Full Power Down Mode : < 70 mW**
- **Package: 44 Pin MQFP (Metric Quad Flat Pack)**

4 - 48



AD9853 and AD8320 in Cable Modems



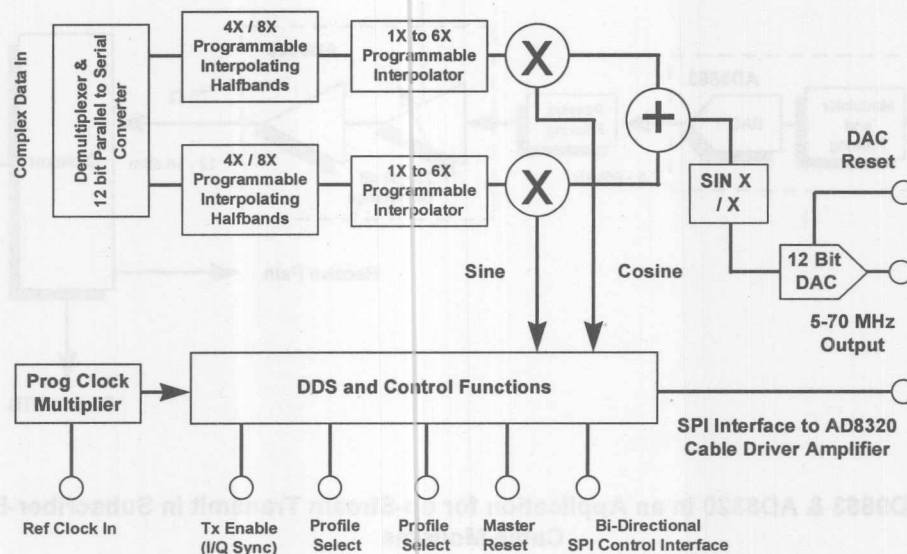
THE AD9853 & AD8320 in an Application for up-Stream Transmit in Subscriber-End Cable Modems

4 - 49



AD9856 200 MHz Quadrature Digital Upconverter

The AD9856 differs from the AD9851 in that it accepts pre-encoded data via a 12 bit parallel input bus.



4 - 50



AD9856 - Key Specs and Features

- **Return Channel Tx Functions : 5 - 70 MHz Output**
- **Frequency Tuning Word: 32-bit Serial Load**
- **180 MHz External Reference Clock Rate**
- **Programmable Reference Clock Multiplier**
- **Programmable Sample Rate Interpolation Filter**
- **Wideband SFDR (Single Tone) : 65 dBc @ 1 MHz, 55 dBc @ 40 MHz**
- **+ 3.3 V Single Supply Operation**
- **Low Power : 400 mW @ Full Clock Speed @ + 3.3V Supply**
- **Full Power Down Mode : 1 mW**
- **Package: 48 Pin TQFP (Thin Quad Flat Pack)**

4-51



AD9886 - Key Specs and Features

- Return Channel Tx Functions: 5-10 MHz Output
- Frequency Tuning Word: 32-bit Serial Load
- 180 MHz External Reference Clock Rate
- Programmable Reference Clock Multiplier
- Programmable Sample Rate Interpolation Filter
- Wideband SDR (Single Tone): 55 dBc @ 1 MHz, 55 dBc @ 40 MHz
- +3.3 V Single Supply Operation
- Low Power: 500 mW @ Full Clock Speed @ +3.3V Supply
- Full Power Down Mode: 1 mW
- Package: 48 Pin TQFP (Thin Quad Flat Pack)

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General Purpose, Single Supply, Low Power D/A Converters



The ADI DAC Family Portfolio...

AD7804, AD7805

**8 Bit Quad Parallel/Serial
2 MHz Multiplying Bandwidth
High Performance**

AD739X Family

**Dual 10/12 Bit
Serial/Parallel
Lowest Power < 100 μ A**

AD53XX Family

**24 Models
8, 10, 12 Bits
Singles, Duals, Quads
Lowest Cost**

4 - 54



AD7304, AD7305 **8 Bit, Quad, Serial/Parallel D/A Converters**

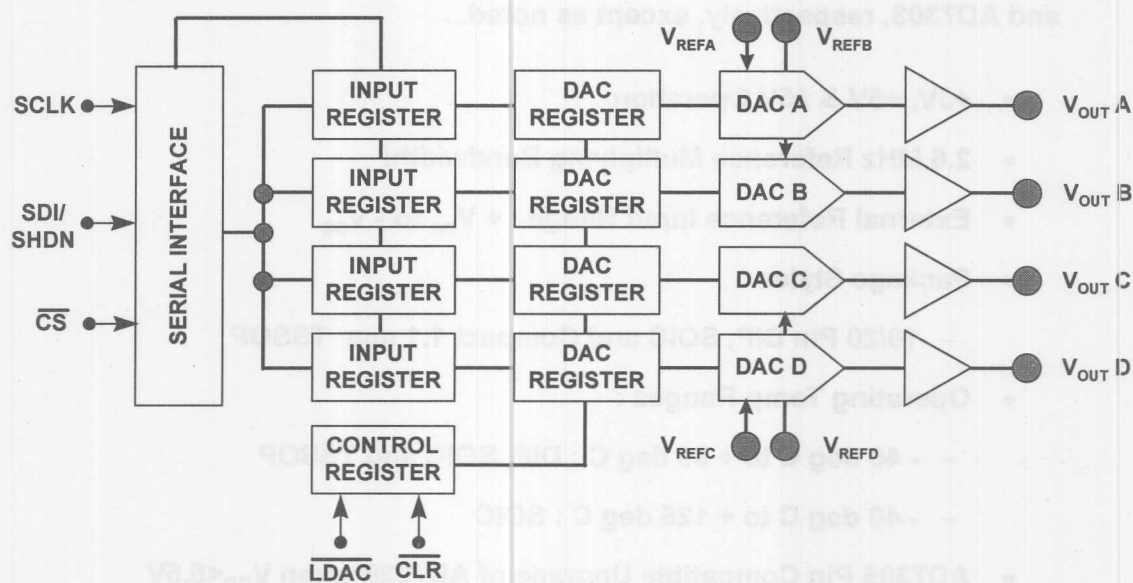
The AD7304 and AD7305 are essentially quad versions of the AD7302 and AD7303, respectively, except as noted...

- **+3V, +5V & ± 5 V Operation**
- **2.6 MHz Reference Multiplying Bandwidth!**
- **External Reference Input Range : + V_{DD} to - V_{SS}**
- **Package Styles :**
 - 16/20 Pin DIP, SOIC and Compact 1.1 mm TSSOP
- **Operating Temp Ranges :**
 - -40 deg C to +85 deg C : DIP, SOIC and TSSOP
 - -40 deg C to +125 deg C : SOIC
- **AD7305 Pin Compatible Upgrade of AD7226 when $V_{DD} < 5.5$ V**

4-55



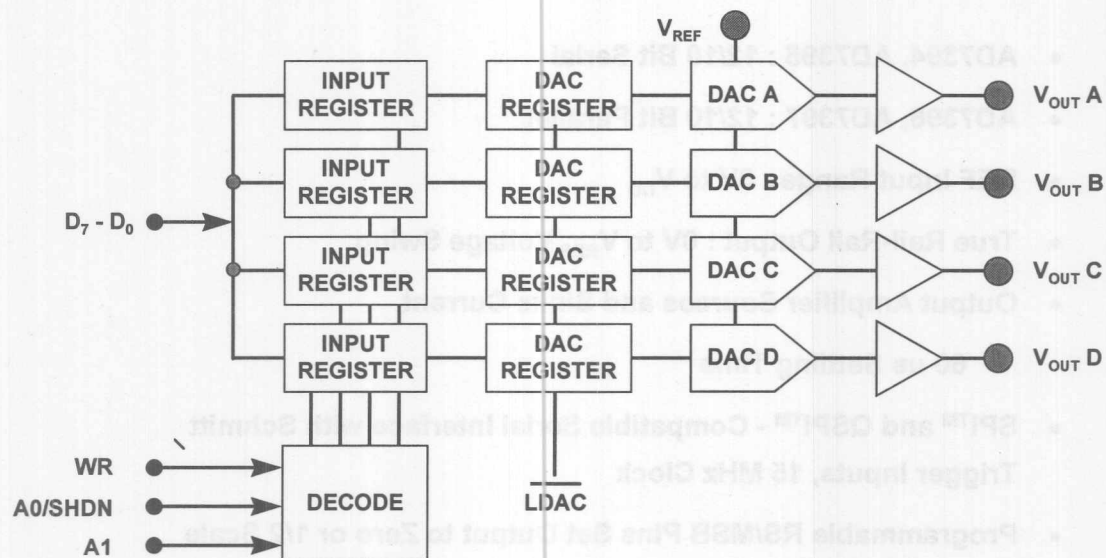
AD7304 - Simplified Diagram



4 - 56



AD7305 - Simplified Diagram



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AD7394-AD7397

10/12-Bit, Dual, Micropower D-A Converters

- **AD7394, AD7395 : 12/10 Bit Serial**
- **AD7396, AD7397 : 12/10 Bit Parallel**
- **REF Input Range : 0V to V_{DD}**
- **True Rail-Rail Output : 0V to V_{REF} Voltage Swing**
- **Output Amplifier Sources and Sinks Current**
 - **60 us Settling Time**
- **SPI™ and QSPI™ - Compatible Serial Interface with Schmitt Trigger Inputs, 15 MHz Clock**
- **Programmable RS/MSB Pins Set Output to Zero or 1/2 Scale**
- **Pin-Programmable SHDN Reduces Supply Current to typ 100 nA**

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AD7394-AD7397 - Key Specs and Features (con't)

- **+ 2.7V to + 5.5V Single Supply Low Operation :**
 - Less Than 200 uA, Normal Operation
 - Typically 0.1 uA Shutdown Current
- **Compact, Low Profile Packaging:**
 - **AD7394/95 :**
 - » 14-Pin DIP, SOIC and 1.1 mm TSSOP-14 (AD7395)
 - **AD7396/97 :**
 - » 24-Pin DIP, SOIC and 1.1 mm TSSOP-24 (AD7397)
- **Operating Temperature Ranges:**
 - DIP, SOIC : -40 deg C to + 85 deg C
 - TSSOP : - 40 deg C to + 125 deg C

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AD53XX Family Micro-Power D/A Converters

Features of the AD53XX Family Include...

- 24 Models to Choose From
- 8, 10 or 12 Bit Resolution
- Single, Dual and Quad Versions
- Versatile 3 Wire, High Speed Serial Interface :
 - 30 MHz Clock Rates, Schmitt-Triggered
 - SPI™, QSPI™, and MICROWIRE™ Compatible
- 2-Wire I²C Interface : 400 kHz

4 - 60



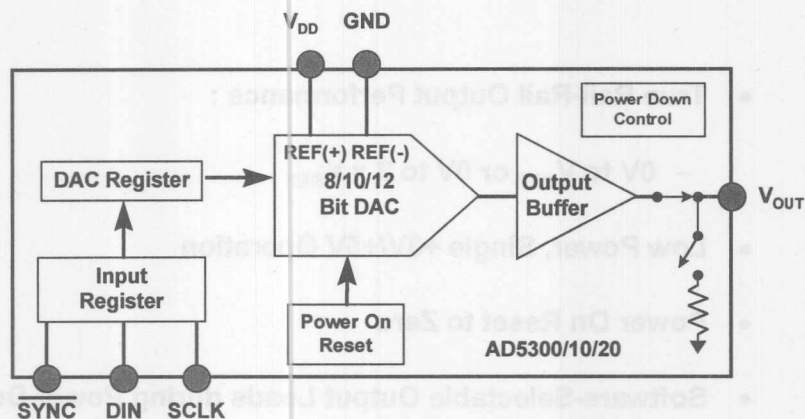
AD53XX Family Features (con't)

- **True Rail-Rail Output Performance :**
 - 0V to V_{REF} or 0V to $2 \times V_{REF}$
- **Low Power, Single +3V/+5V Operation**
- **Power On Reset to Zero**
- **Software-Selectable Output Loads during Power Down**
- **-40 deg C to +105 deg C Temperature Range**
- **Pin-Pin Compatibility**

4 - 61



AD5300, AD5310 and AD5320 8/10/12 Bit, Rail-Rail Serial D/A Converters



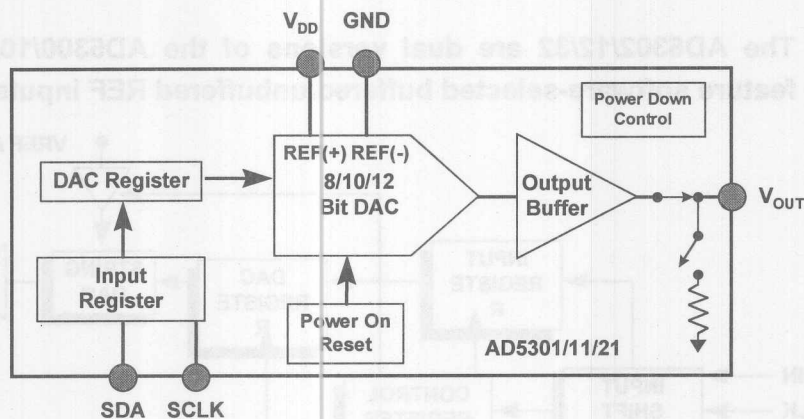
- High Speed 3-Wire Serial Interface
- 0V to V_{REF} Output Range
- 5V @ 250 uA, 1 uA in POWER DOWN mode
- 6 Pin SOT (AD5300) and 8 Pin uSOIC Packages

4 - 62



Preliminary
Information

AD5301*, AD5311* and AD5321* 8/10/12 Bit, Rail-Rail Serial D/A Converters



- Same Specifications as AD5300/10/20
- 2-Wire, I²C Interface

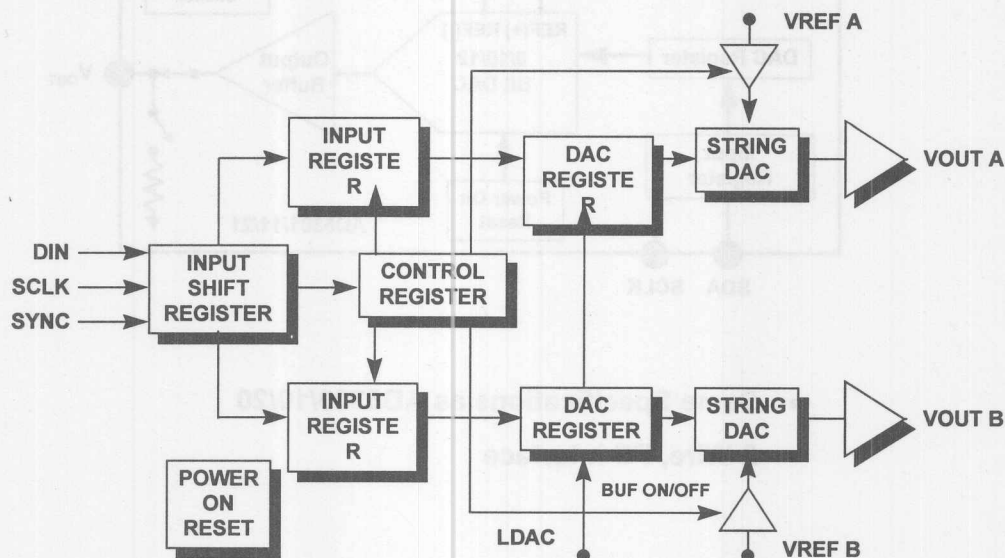
4-63



Preliminary
Information

AD5302*, AD5312* and AD5322* 8/10/12 Bit, Dual, Rail-Rail D/A Converters

The AD5302/12/32 are dual versions of the AD5300/10/20 and feature software-selected buffered/unbuffered REF inputs



4-64



AD5302/12/22 - 16 Bit Serial Input Word Shift Register

DB15 (MSB)

← DATA BITS →

DB0 (LSB)

AD5302

A/B	BUF	PD1	PD0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
-----	-----	-----	-----	----	----	----	----	----	----	----	----	---	---	---	---

AD5312

A/B	BUF	PD1	PD0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----	---	---

AD5322

A/B	BUF	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----



AD5302/12/22 - 16 Bit Shift Register Control Bits

- **A/B** : Controls Which DAC is Written To:
 - 0 : Data Written to DAC A
 - 1 : Data Written to DAC B
- **BUF** : Controls Buffered or Unbuffered Operation of Reference
 - 0 : Unbuffered
 - 1 : Buffered
- **Power Down Bits** (see below)

PD1	PD0	Operating Mode
0	0	Normal Operation
0	1	Power Down (1 k Ω load to GND)
1	0	Power Down (100 k Ω load to GND)
1	1	Power Down (Hi-Z Output)

4-66



AD5303, AD5313 and AD5323 8/10/12 Bit, Dual, Rail-Rail D/A Converters

The AD5303, AD5313 and AD5323 are identical in performance to the AD5302, AD5312 and AD5322, respectively, with the following differences:

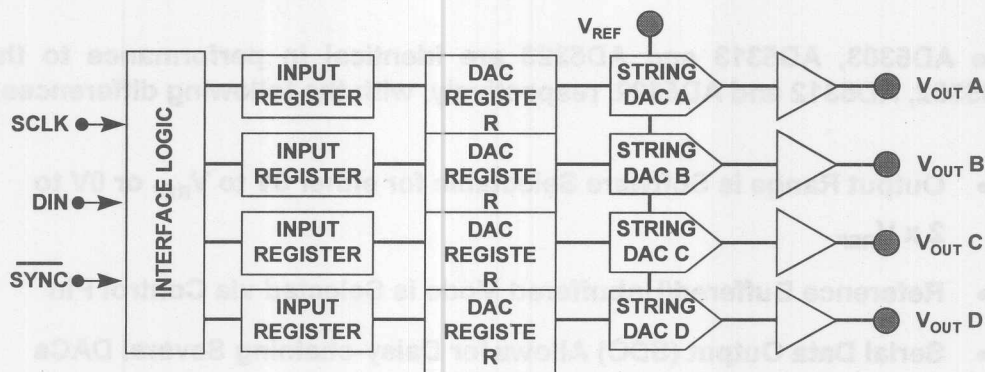
- Output Range is Software Selectable for either 0V to V_{REF} or 0V to $2 \times V_{REF}$
- Reference Buffered/Unbuffered Mode is Selected via Control Pin
- Serial Data Output (SDO) Allows for Daisy-chaining Several DACs
- PD Pin provides Additional Hardware Control of Power Down Mode
- CLR (clear) Pin Resets DAC and Input Registers to Zero
- 16 Pin TSSOP Package

4-67



Preliminary
Information

AD5304*, AD5314* and AD5324* 8/10/12 Bit Quad Rail-Rail D/A Converters



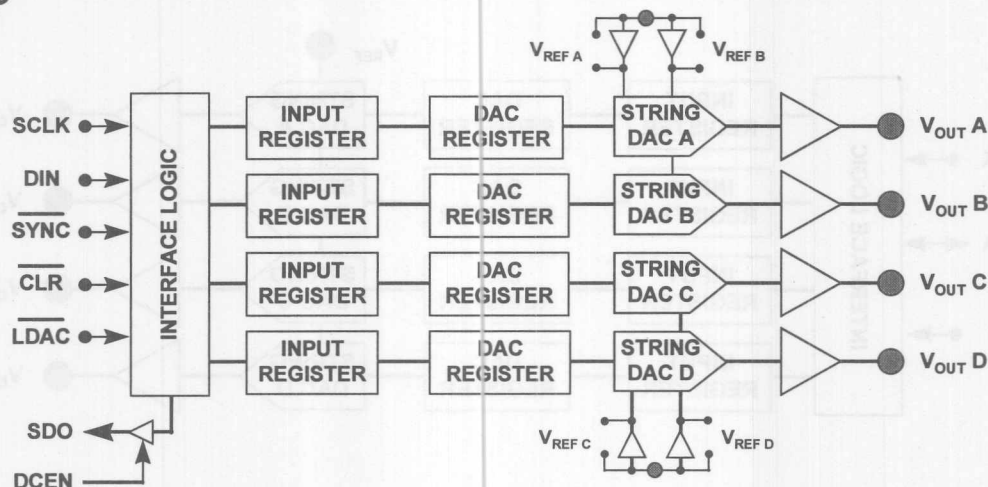
- High Speed 3-Wire Serial Interface
- 0V to V_{REF} Output Range
- 3V @ 500 μ A, 50 nA in POWER DOWN mode
- 10 Pin uSOIC Package

4-68



Preliminary
Information

AD5307*, AD5317* and AD5327* 8/10/12 Bit Quad Rail-Rail D/A Converters



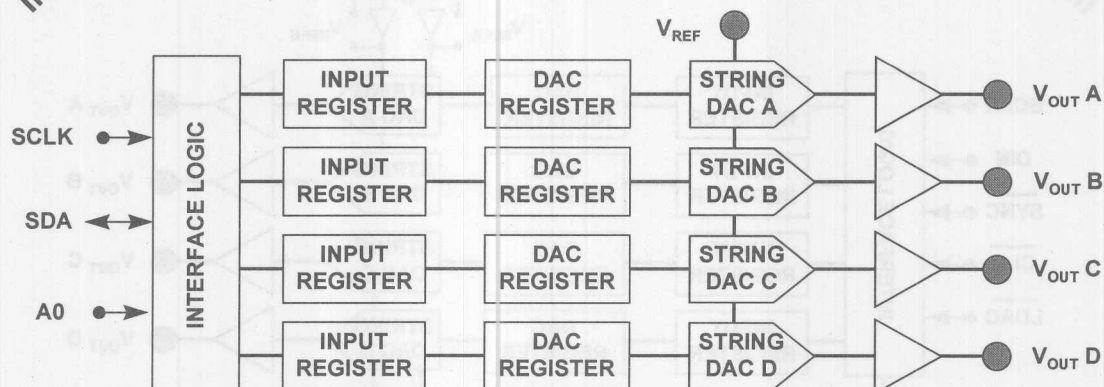
- Same Specifications as AD53X4 Series
- Daisy Chain Capability (SDO)
- DCEN Function
- 2 Reference Inputs, Buffered Unbuffered Modes
- Power Down (PD) Logic Pin
- 16 Pin TSSOP Package

4-69



Preliminary
Information

AD5305*, AD5315* and AD5325* 8/10/12 Bit Quad Rail-Rail D/A Converters



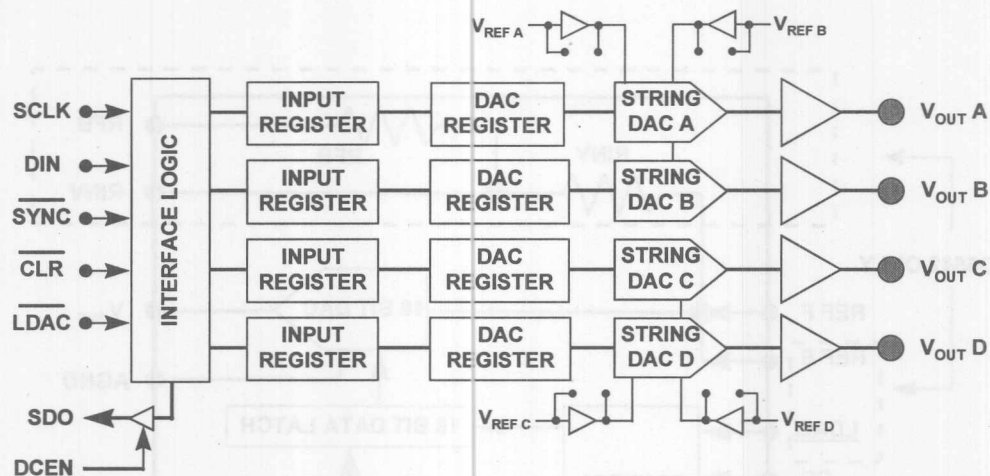
- Same Specifications as AD53X4 Series
- 2-Wire, I²C Interface
- 10 Pin uSOIC Package

4 - 70



Preliminary
Information

AD5306*, AD5316* and AD5326* 8/10/12 Bit Quad Rail-Rail D/A Converters



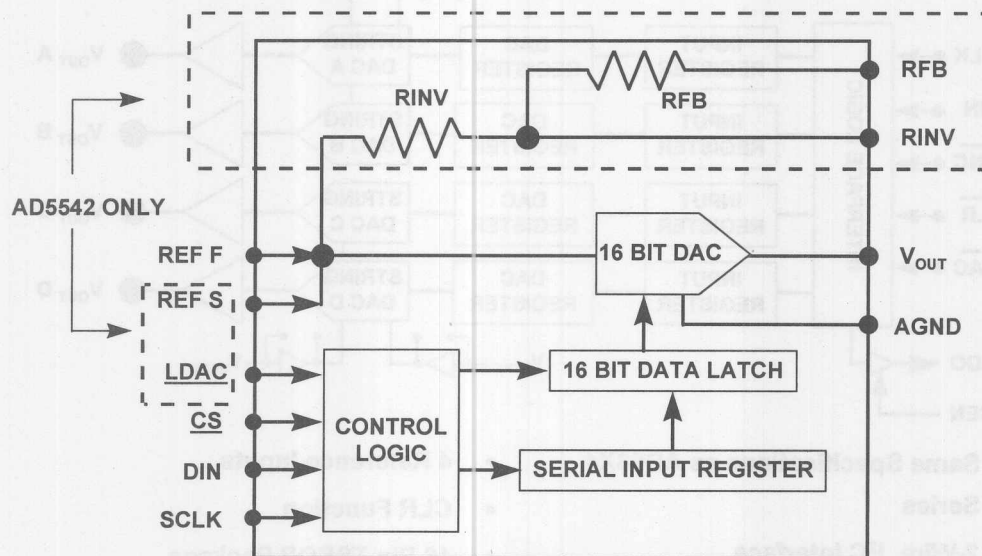
- Same Specifications as AD53X4 Series
- 2-Wire, I²C Interface
- Output Range 0- V_{REF} or 0- $2V_{REF}$
- 4 Reference Inputs
- CLR Function
- 16 Pin TSSOP Package

4-71



Preliminary
Information

AD5541* and AD5542* 16 Bit Voltage Output D/A Converters



4-72



AD5541, AD5542 - Key Specs and Features

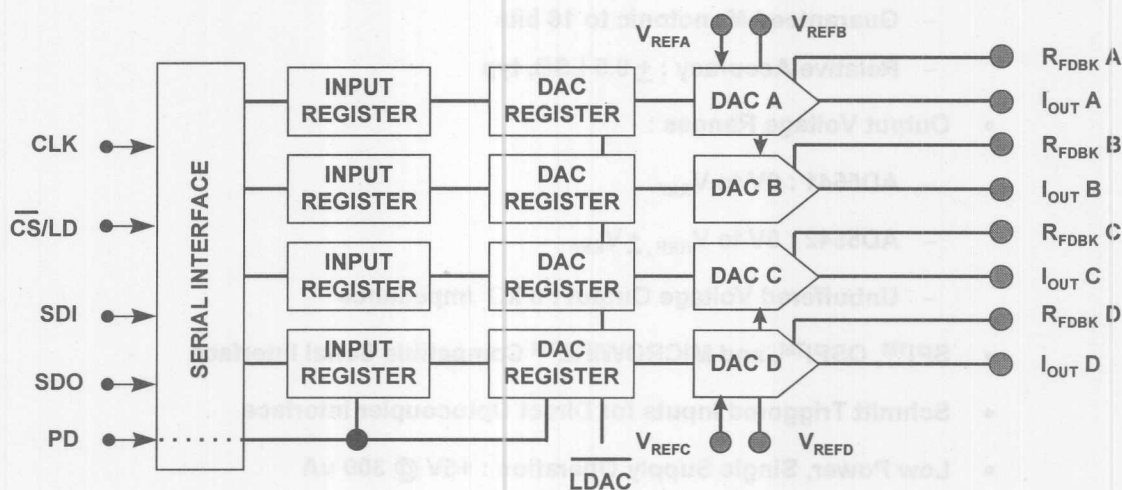
- True 16 Bit Performance :
 - Guaranteed Monotonic to 16 bits
 - Relative Accuracy : ± 0.5 LSB, typ
- Output Voltage Ranges :
 - AD5541 : 0V to V_{REF}
 - AD5542 : 0V to $V_{REF}, \pm V_{REF}$
 - Unbuffered Voltage Output : 6 k Ω Impedance
- SPI™, QSPI™, and MICROWIRE™ Compatible Serial Interface
- Schmitt Triggered Inputs for Direct Optocoupler Interface
- Low Power, Single Supply Operation : +5V @ 300 uA
- Power-On Reset Clears DAC Output to Zero Volts (Unipolar Mode)
- 8/14 Pin DIP and SOIC Package Types

4 - 73



Preliminary
Information

AD5544* 16 Bit, Quad Current Output D/A Converter



4-74



AD5544 - Key Specs and Features

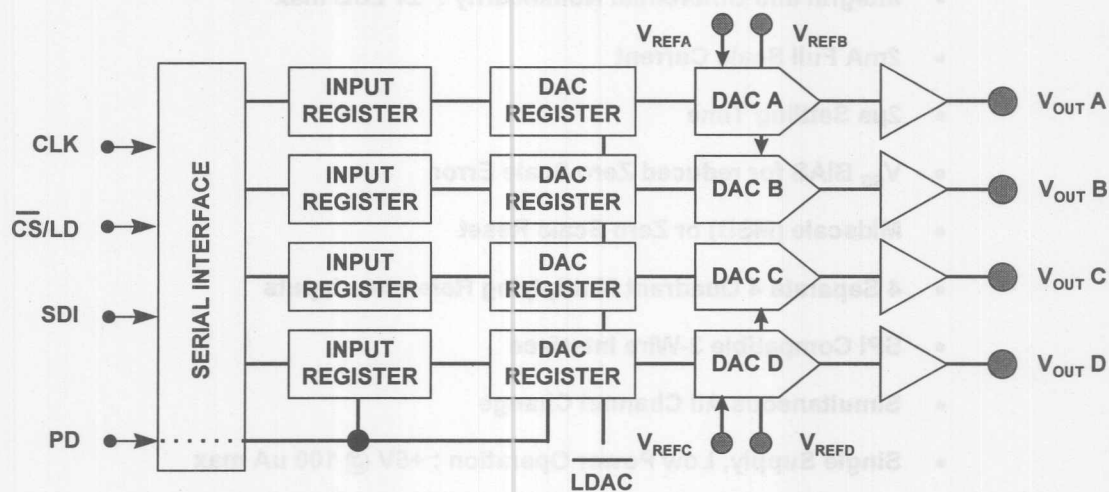
- Integral and Differential Nonlinearity : ± 1 LSB max
- 2mA Full Scale Current
- 2 μ s Settling Time
- V_{SS} BIAS for reduced Zero Scale Error
- Midscale (MSB) or Zero Scale Reset
- 4 Separate 4 Quadrant Multiplying Reference Inputs
- SPI Compatible 3-Wire Interface
- Simultaneous All Channel Change
- Single Supply, Low Power Operation : +5V @ 100 μ A max
- Internal Power ON Reset
- Compact SSOP-28 Package

4-75

Preliminary
Information

AD7398*

Quad, Serial Input, 12 Bit D/A Converter



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AD7398 - Key Specs and Features

- 3 Wire SPI™, QSPI™, and MICROWIRE™ Compatible

Serial Interface

- Single + 5V or Dual \pm 5V Operation :
 - Only 250 uA per DAC
- Separate Reference Inputs
- Programmable Power Down Mode
- Internal Power On Reset
- 16 Pin DIP, SOIC and Compact 1.1 mm Height TSSOP

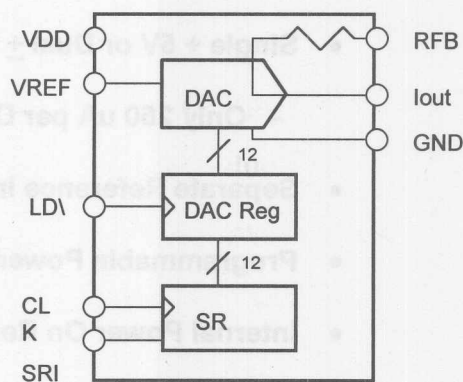
Packages

4-77



DAC8043A 12-Bit 4 Quadrant Multiplying D/A Converter

- + 5V Operation @ <10uA
- Fast 3-Wire Serial Input
- Fast 1 μ s Settling Time
- >1MHz 4-Quadrant Multiply BW
- Pin-for-Pin Upgrade for DAC8043
- Standard Pin Out
- Compact 8-Pin SOIC & TSSOP Packages



4-78



Preliminary
Information

AD7839 * 13 Bit Octal D/A Converter

The AD7839 contains eight 13-bit D/A Converters in one package!

- Buffered Voltage Outputs : $\pm 10V$
- Independent Offset Adjustment for Each DAC Pair
- Requires $\pm 15V$ and $+ 5V$ Supplies
- Double Buffered Digital Inputs
- Asynchronous LOAD and CLEAR Facilities
- Fast 5 μs Settling Time
- Controlled Power ON of Output Stage
- Separate Reference Inputs
- Compact 44-Pin PQFP Package

4 - 79



AD7838 13 Bit Octal D/A Converter

The AD7838 is an improved second source to the MAX547

- **Buffered Voltage Outputs : $\pm 4.5V$**
- **Requires $\pm 5V$ Supplies**
- **Double Buffered Digital Inputs**
- **Asynchronous LOAD and CLEAR Facilities**
- **Fast 5 μs Settling Time**
- **Controlled Power ON of Output Stage**
- **Separate Reference Inputs : $\pm 5V$**
- **Compact 44-Pin PLCC Package**

4 - 80



**Preliminary
Information**

AD7841*
Octal 14 Bit D/A Converter

- **Buffered Voltage Outputs : $\pm 10V$**
- **Independent Offset Adjustment for Each DAC Pair**
- **$\pm 10.8V$ to $\pm 16.5V$ Supplies**
- **Double Buffered Digital Inputs**
- **Asynchronous LOAD and CLEAR Facilities**
- **Fast 20 μs Settling Time**
- **Separate Reference Inputs : $\pm 5V$**
- **Compact 44-Pin PQFP Package**

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Digital Potentiometers

- Compact 4-Pin PDIP Package
- Separate Reference Inputs : $\pm 5V$
- Fast 50 μs Settling Time
- Asynchronous LOAD and CLEAR Facilities
- Double Buffered Digital Inputs
- ± 10 mV Resolution
- Independent Offset Adjustment for Each DAC Pair
- Buffered Voltage Outputs : $\pm 10V$

4 - 82



AD5203

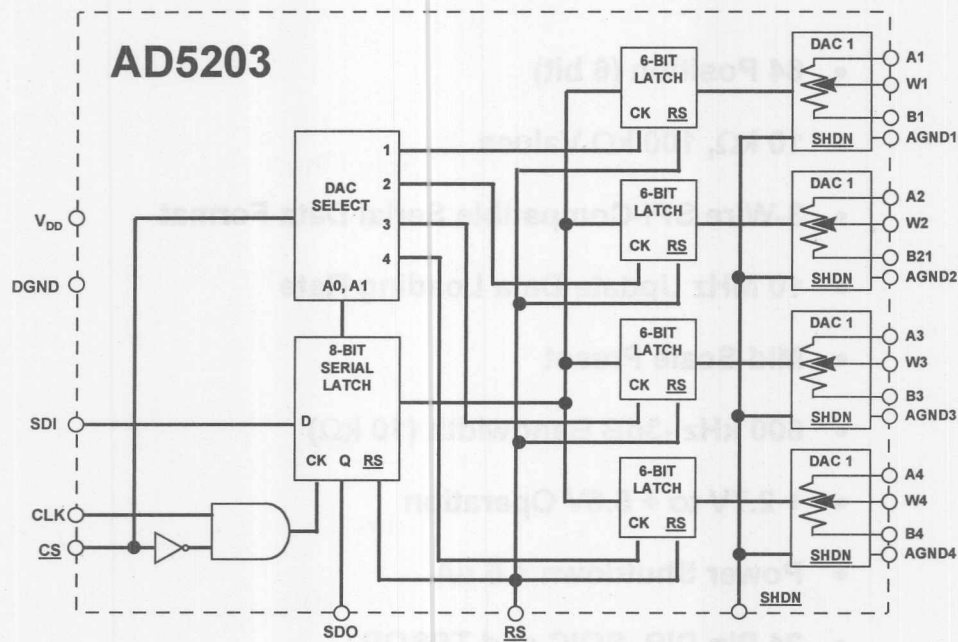
4 Channel, 64 Position Digital Potentiometer

- 64 Position (6 bit)
- 10 k Ω , 100 k Ω Values
- 3-Wire SPI-Compatible Serial Data Format
- 10 MHz Update Data Loading Rate
- Mid-Scale Preset
- 600 kHz -3dB Bandwidth (10 k Ω)
- + 2.7V to + 5.5V Operation
- Power Shutdown < 5 μ A
- 24 Pin DIP, SOIC and TSSOP

4 - 83



AD5203 Block Diagram



4-84



**Preliminary
Information**

AD5204*, AD5206* 4/6 Channel Digital Potentiometers

- **256 Position (8 Bits)**
- **4/6 Independently Programmable Channels**
- **10 k Ω , 50 k Ω and 100 k Ω Values**
- **3-Wire SPI-Compatible Serial Data Input**
- **600 kHz - 3dB Bandwidth (10 k Ω)**
- **Single/Dual Supply Operation : + 3V to + 5V, \pm 2.5V**
- **- 40 deg C to + 85 deg C Operation**
- **24 Pin DIP, SOIC and TSSOP Packages**

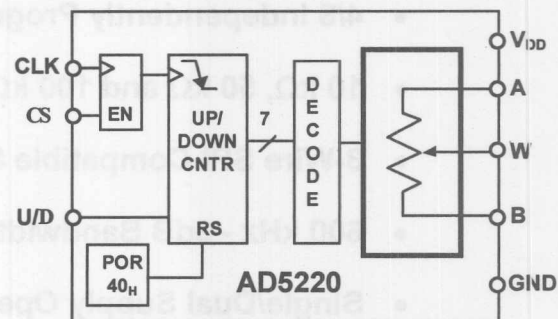
4 - 85



Preliminary
Information

AD5220*, AD5222* Increment/Decrement Digital Potentiometers

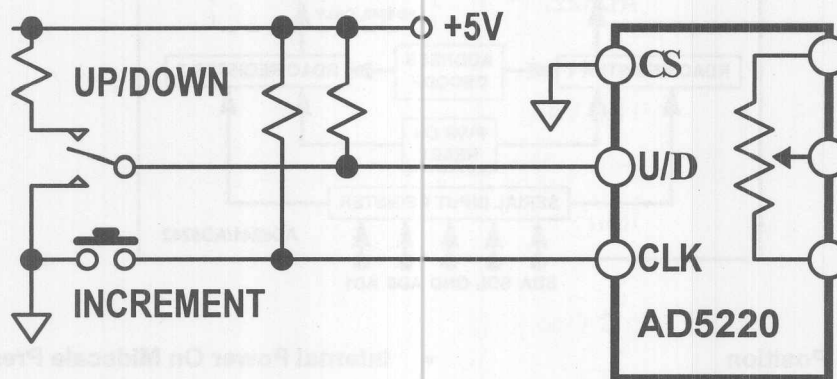
- AD5220 (single) and AD5222 (dual)
- 128 Position (7 Bits)
- 10 k Ω , 50 k Ω and 100 k Ω Values
- 650 kHz - 3dB Bandwidth (10 k Ω)
- Single Supply Operation : + 2.7V to + 5.5V
- - 40 deg C to + 85 deg C Operation
- 8 Pin DIP, SOIC and uSOIC Packages



4 - 86



Typical Push-Button Control Application

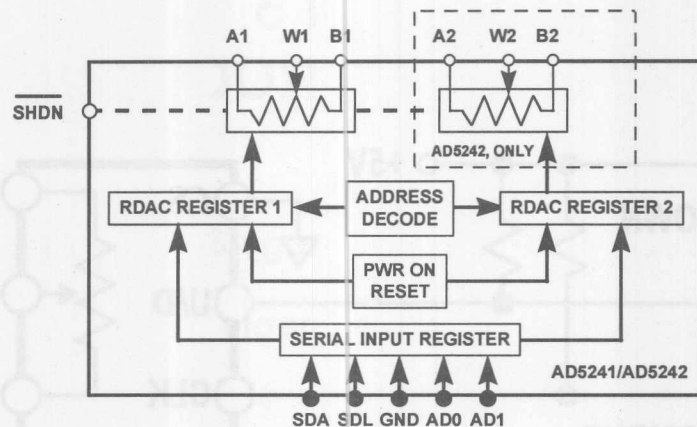


4 - 87



Preliminary
Information

AD5241*, AD5242* I²C-Compatible Digital Potentiometers



- 256 Position
- 10K, 50K and 100K ohm Versions
- 650 kHz BW (10K ohms)
- Shutdown Mode : B-W short, A open circuit
- Internal Power On Midscale Preset
- Single/Dual Power Supply Range :
 - 2.7V p-p to 5.5V p-p, 5 uA max
- 14 Pin SOIC and TSSOP Packages

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SECTION 5

DIGITAL SIGNAL PROCESSING

- **DSP Core Technology Strategy & Roadmaps**
- **General-purpose Programmable DSPs**
- **Embedded DSP Solutions**
- **Development Tools from ADI & Partners**
- **Systems and Solutions**



SECTION 5 DIGITAL SIGNAL PROCESSING

- DSP Core Technology Strategy & Roadmaps
- General-purpose Programmable DSPs
- Embedded DSP Solutions
- Development Tools from ADI & Partners
- Systems and Solutions

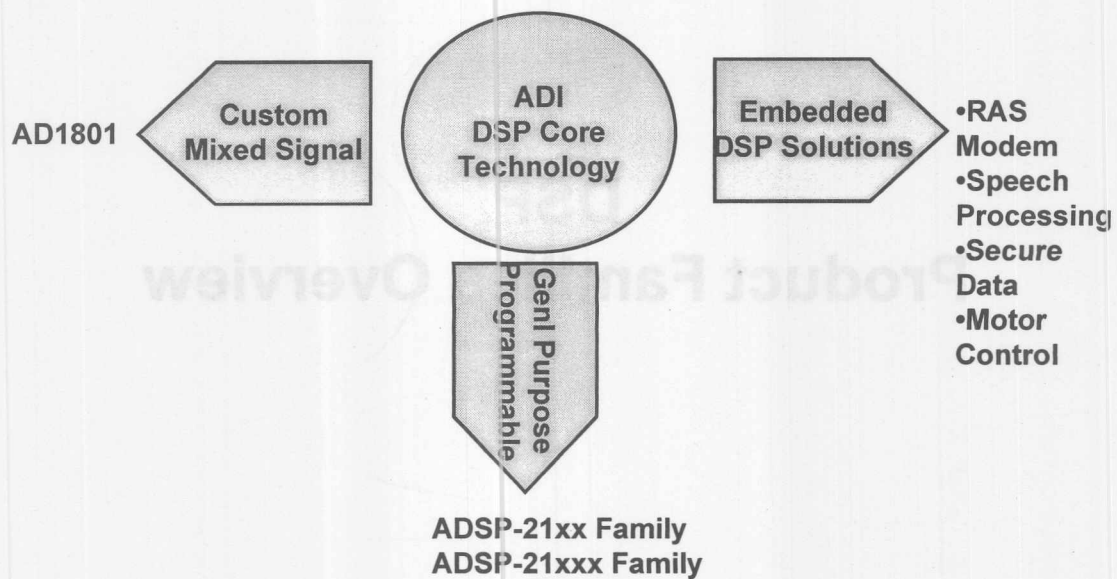


DSP

Product Families Overview

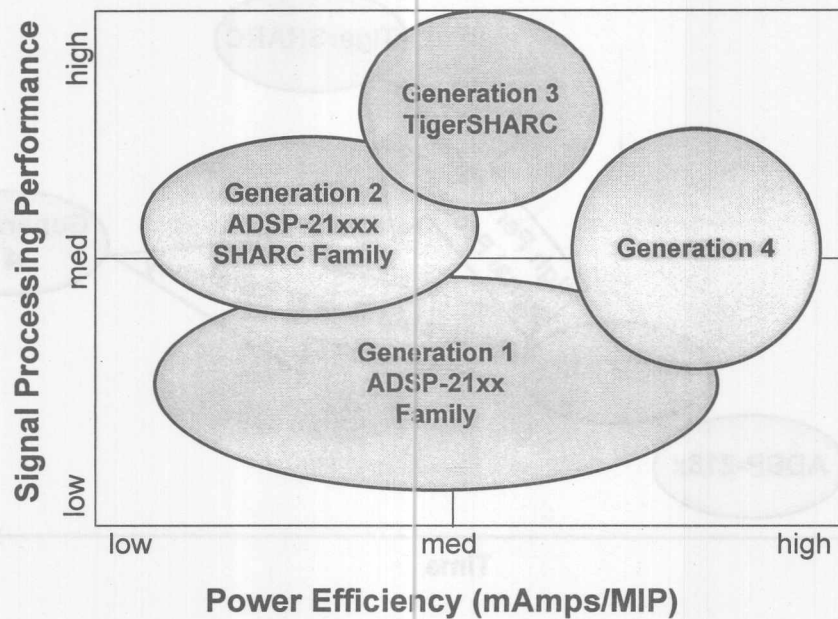


ADI DSP Strategy





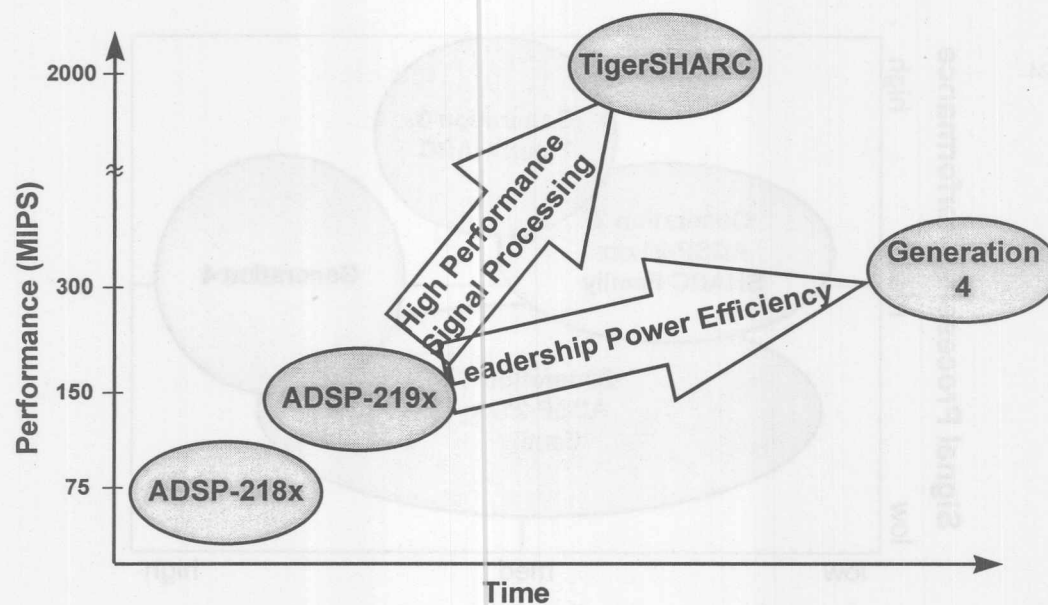
30 Years of Signal Processing: 4 Generations of ADI DSP



5



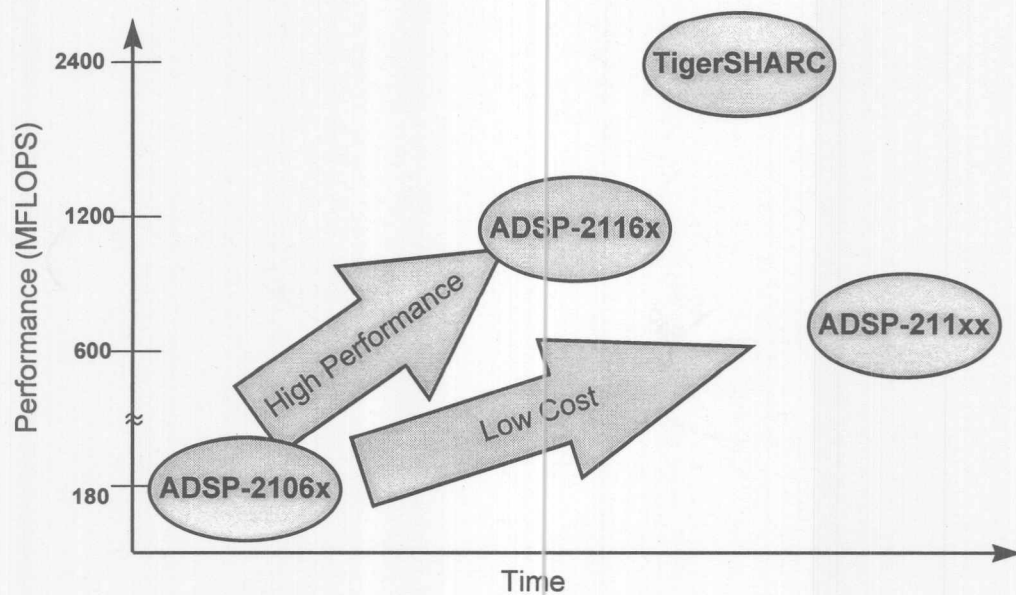
ADI 16-bit DSP Roadmap



6



ADI 32-bit DSP Roadmap



7





General-Purpose, Programmable Digital Signal Processors

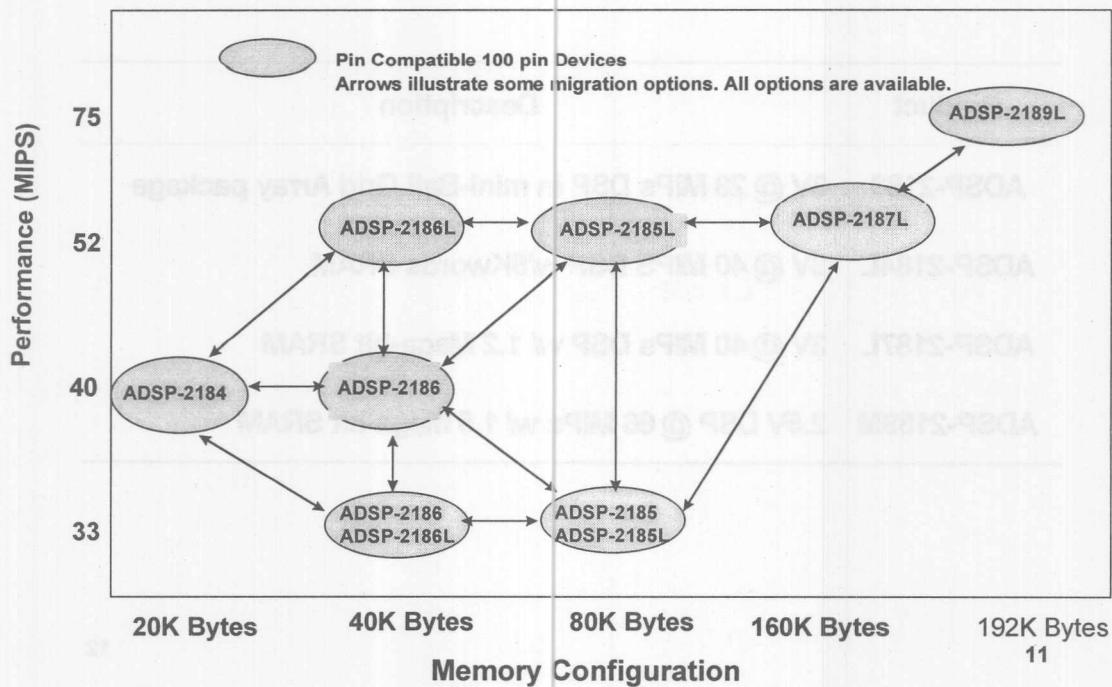


New ADSP-218x Family Members

- **ADSP-2183 : mini-BGA, World's Smallest DSP**
- **ADSP-2184: Lowest Cost 218x**
- **ADSP-2187L : 160 Megabytes SRAM @ 52 MHz**
- **ADSP-2189L : 192 KBytes SRAM @ 75 MHz**



ADSP-218X Family Provides a Pin Compatible Migration Path





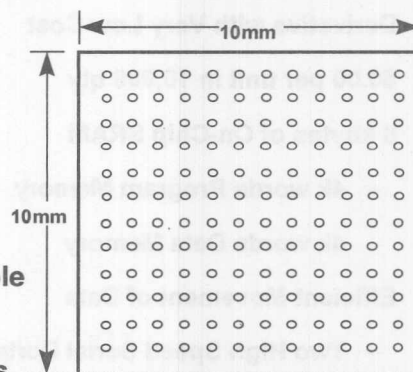
Newest Members of the 218x Family

Product	Description
ADSP-2183	3V @ 29 MIPS DSP in mini-Ball Grid Array package
ADSP-2184L	3V @ 40 MIPS DSP w/8Kwords SRAM
ADSP-2187L	3V @ 40 MIPS DSP w/ 1.2 Mega-bit SRAM
ADSP-2189M	2.5V DSP @ 66 MIPS w/ 1.5 Mega-bit SRAM



ADSP-2183 mini BGA - The World's Smallest DSP!

- Mini-Ball Grid Array Package - 52 MIPS in 1cm²
- Small Size With No Compromises in Performance
 - 144-Pin Package
 - 160Kbytes on-Chip SRAM
- Innovative Packaging for Highly Portable Applications
- Package Size at 0.8 mA Per MIP Targets Handheld Battery-Powered Applications
- Designing with BGA's:
<http://www.analog.com/dsp/bga/>

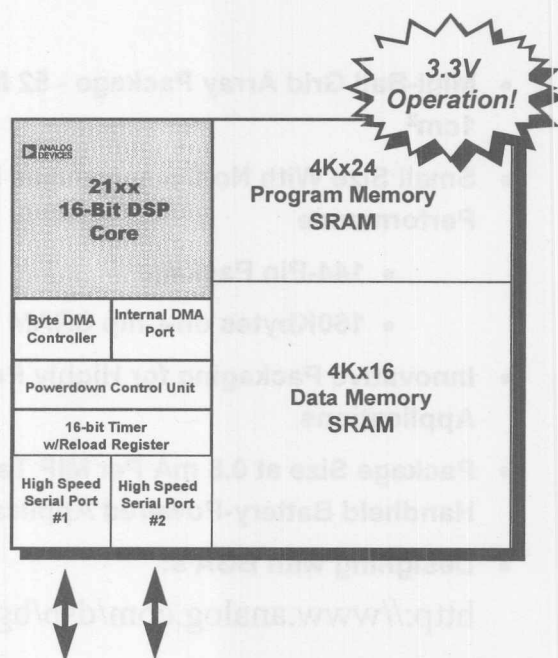


Chip Array Package
144-ball array



ADSP-2184L - Lowest Cost 218x

- Code-Compatible ADSP-218X Derivative with Very Low Cost
- \$6.00 per unit in 10,000 qty
- 8 kbytes of On-Chip SRAM
 - 4k words Program Memory
 - 4k words Data Memory
- Efficient Movement of Data
 - Two High Speed Serial Ports
 - Two DMA Subsystems
- 100 Pin TQFP Is Pin-Compatible With Previous 218X Family Devices

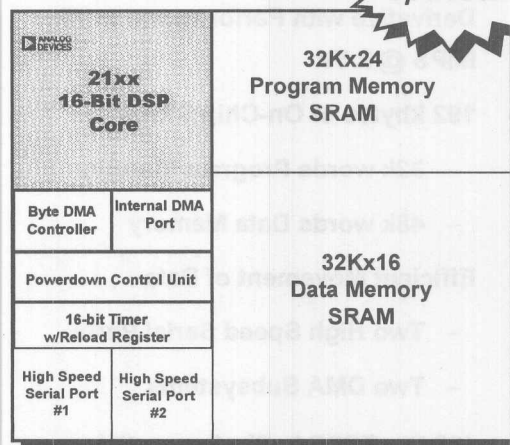


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ADSP-2187L - 160Kbytes SRAM @ 52MIPS

- Code-Compatible ADSP-218X Derivative with Performance to 52 MIPS @ 3.3V
- 160 kbytes of On-Chip SRAM
 - 32k words Program Memory
 - 32k words Data Memory
- Efficient Movement of Data
 - Two High Speed Serial Ports
 - Two DMA Subsystems
- 100 Pin TQFP Is Pin-Compatible With Previous 218X Family Devices
- 312MIPS MCM Also Available

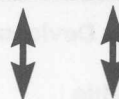
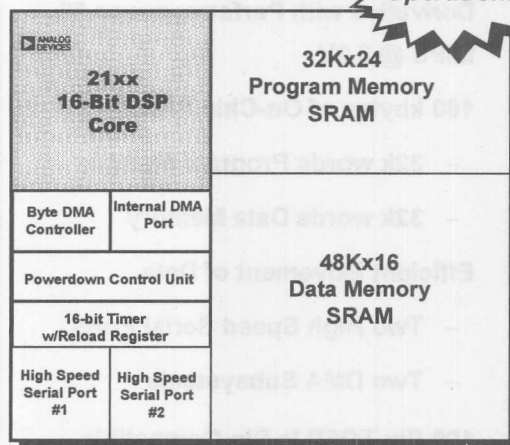


15



ADSP-2189L - 192Kbytes SRAM @ 75MIPS

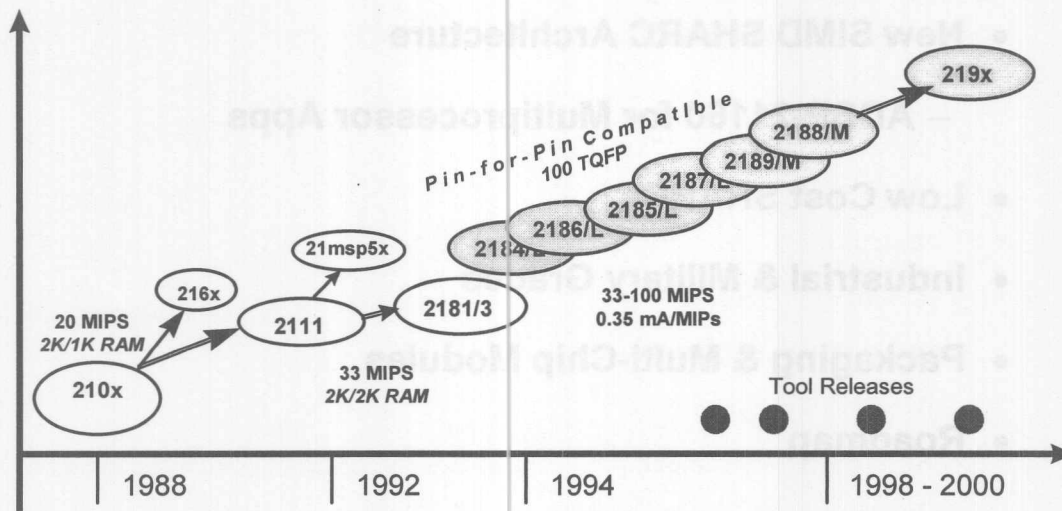
- Code-Compatible ADSP-218X Derivative with Performance to 75 MIPS @ 2.5V
- 192 kbytes of On-Chip SRAM
 - 32k words Program Memory
 - 48k words Data Memory
- Efficient Movement of Data
 - Two High Speed Serial Ports
 - Two DMA Subsystems
- 100 Pin TQFP Is Pin-Compatible With Previous 218X Family Devices



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Code Compatible, 16-bit DSP Roadmap





Newest ADSP-21xxx SHARC Digital Signal Processors

- New SIMD SHARC Architecture
 - ADSP-21160 for Multiprocessor Apps
- Low Cost SHARCs
- Industrial & Military Grades
- Packaging & Multi-Chip Modules
- Roadmap

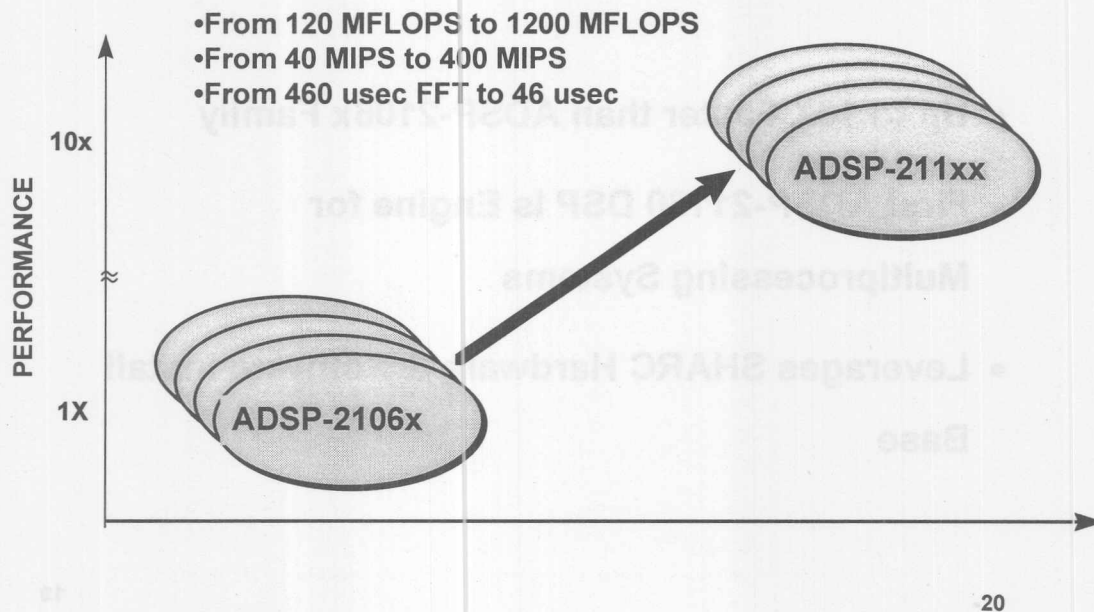


New SIMD SHARC: ADSP-21100 Family Preserves Code Investment

- **Up to 10X Faster than ADSP-2106x Family**
- **First ADSP-21160 DSP Is Engine for
Multiprocessing Systems**
- **Leverages SHARC Hardware & Software Install
Base**

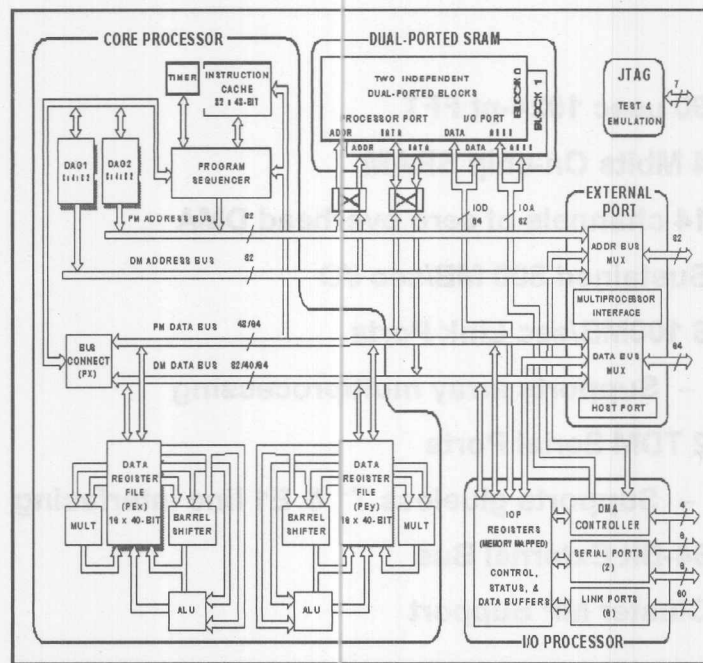


ADSP-211xx SHARC Family Provides 10X Performance Increase





ADSP 21160 Block Diagram



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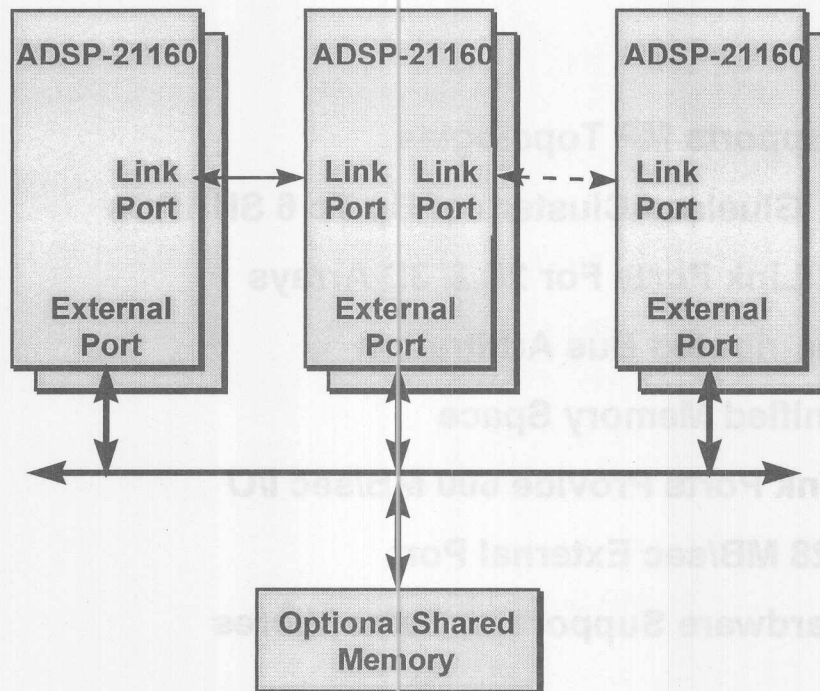
ADSP 21160

- **90 μ sec 1024-pt FFT**
- **4 Mbits On-chip SRAM**
- **14 channels of zero overhead DMA**
- **Sustained 800 MB/sec I/O**
- **6 100MB/sec Link Ports**
 - **Supports array multiprocessing**
- **2 TDM Serial Ports**
 - **Supports glueless T1 & E1 line interfacing**
- **64-Bit External Bus**
- **Cluster MP Support**

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ADSP-21160: MP Engine By Design



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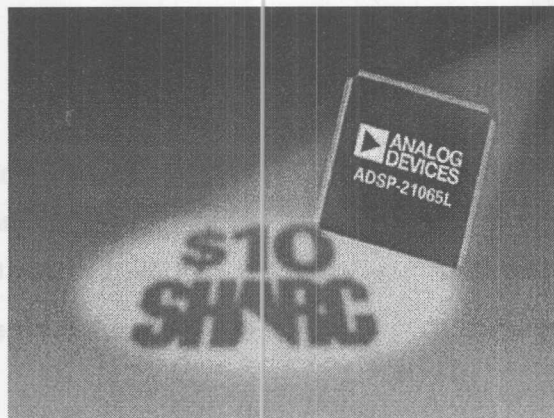
ADSP-21160: MP Engine By Design

- **Supports MP Topologies**
 - **Glueless Clusters of Up To 6 SHARCs**
 - **Link Ports For 2D & 3D Arrays**
- **Distributed Bus Arbitration**
- **Unified Memory Space**
- **Link Ports Provide 600 MB/sec I/O**
- **528 MB/sec External Port**
- **Hardware Support for Semaphores**

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ADSP-21065L: New \$10 SHARC DSP



- **High performance SHARC DSP**
- **Targets Fixed-point & Floating-point Applications**
- **Brings 32-bit precision and floating-point ease of use to real-time embedded systems**

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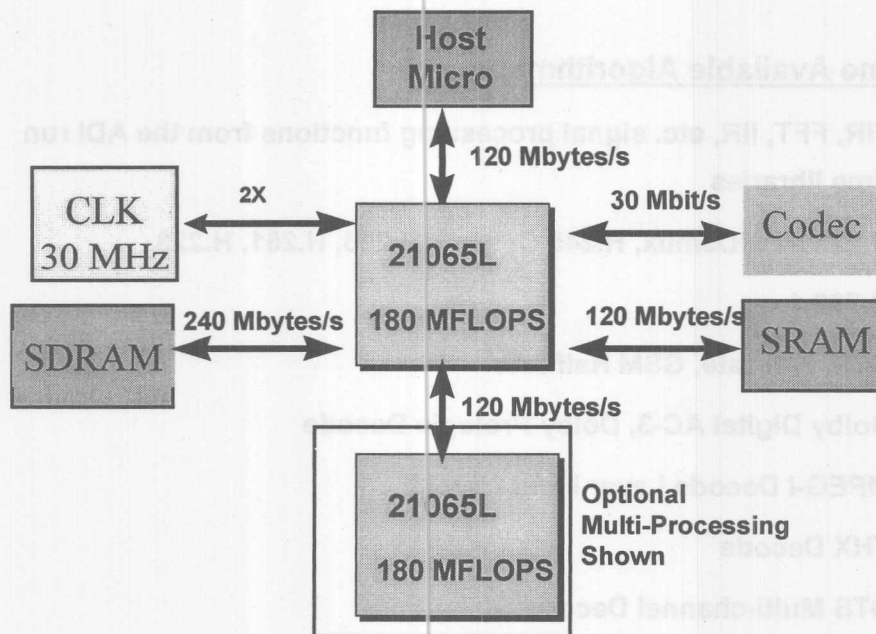


ADSP-21065L: Target Applications

- **Speech Recognition**
 - Computer, Medical, Industrial, Communications
- **Smart Phones**
- **Telecom Infrastructure**
 - PBX, WLL, Central Office
- **Biometrics**
- **Computer Telephony**
- **Automotive**
 - Smart Airbags, Collision Avoidance/Cruise Control, In-Cabin Entertainment
- **Industrial & Instrumentation**
- **Digital Audio**
 - Digital Speakers, Pro Audio, Prosumer, Home Theater



ADSP-21065L: Optimized Core, Memory & I/O



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ADSP-21065L Offers Code Compatibility for Fast Time To Market

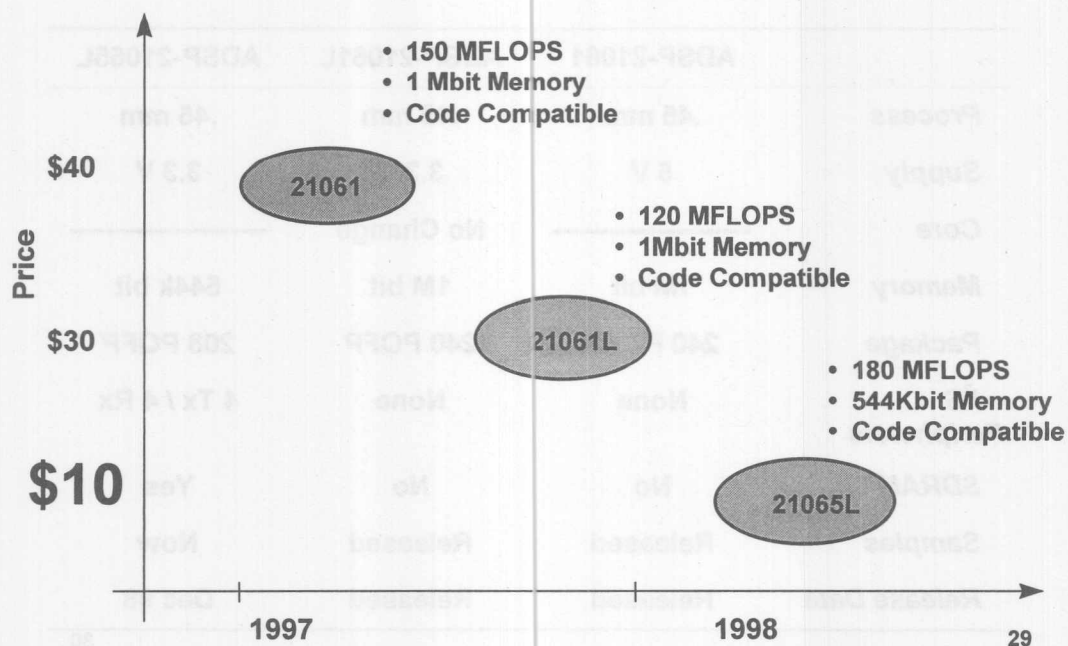
Some Available Algorithms:

- **FIR, FFT, IIR, etc. signal processing functions from the ADI run time libraries**
- **H.223 Mux/Demux, H.245 Control, H.263, H.261, H.223**
- **G.723.1**
- **GSM Full-rate, GSM Half-rate**
- **Dolby Digital AC-3, Dolby Prologic Decode**
- **MPEG-I Decode Layer I and Layer II**
- **THX Decode**
- **DTS Multi-channel Decode**

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Lowering the Cost of SHARC DSPs





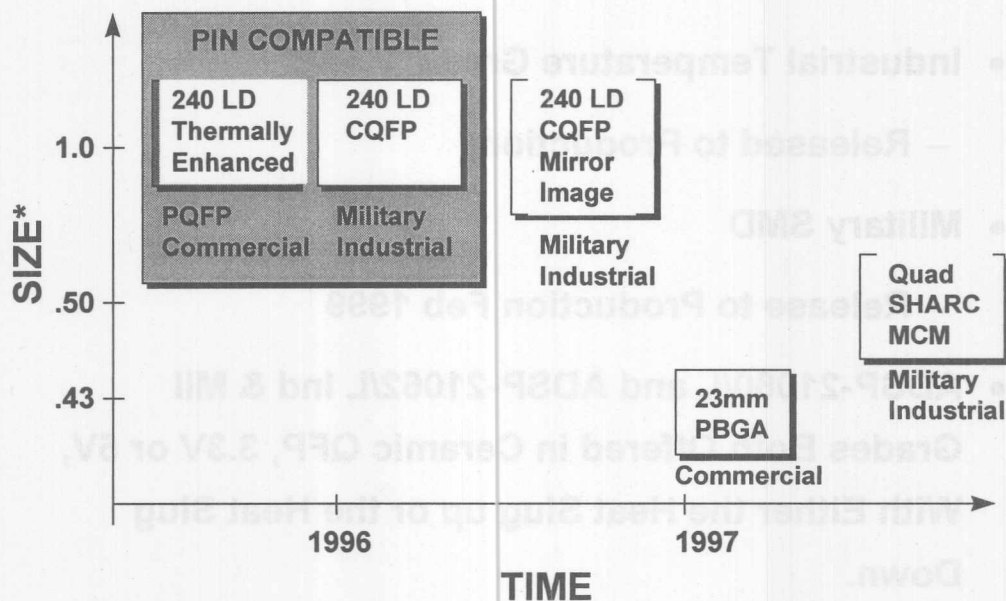
Low Cost SHARC Features

	ADSP-21061	ADSP-21061L	ADSP-21065L
<i>Process</i>	.45 mm	.45 mm	.45 mm
<i>Supply</i>	5 V	3.3 V	3.3 V
<i>Core</i>	-----	No Change	-----
<i>Memory</i>	1M bit	1M bit	544k bit
<i>Package</i>	240 PQFP	240 PQFP	208 PQFP
<i>I²S</i>	None	None	4 Tx / 4 Rx
<i>Peripherals</i>			
<i>SDRAM I/F</i>	No	No	Yes
<i>Samples</i>	Released	Released	Now
<i>Release Date</i>	Released	Released	Dec 98

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SHARC Packaging Roadmap



* Normalized to 240 LD PQFP and one processor

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Industrial Temperature and Military SMD SHARCs

- **Industrial Temperature Grade**
 - Released to Production
- **Military SMD**
 - Release to Production Feb 1999
- **ADSP-21060/L and ADSP-21062/L Ind & Mil**
Grades Both Offered in Ceramic QFP, 3.3V or 5V,
With Either the Heat Slug up or the Heat Slug
Down.

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Quad SHARC MCM (Multi-Chip Module)

- **Quad 21060 Cluster With Common External Bus**
- **40MHz Operation Over Industrial and Mil Temperatures**
- **47mm Square Package, .200" Max. Height**
- **Qualification and Screening to MIL-STD-883**

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DSP MCM Products from ADI

The AD14160 and AD14160 are fully integrated, *performance enhanced*, multichip modules targeted at high reliability, performance/density driven applications

AD14060:

- Quad-21060 module in CQFP
- 480 MFLOPS
- 12 link ports, 5 serial ports

AD14160:

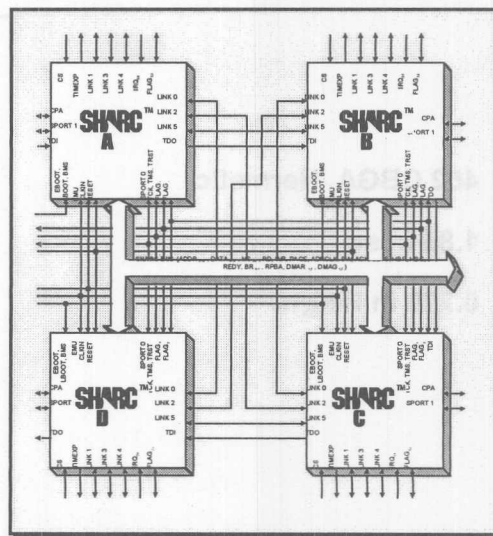
- Quad-21060 module in CBGA
- 480 MFLOPS
- 16 link ports, 8 serial ports



AD14060 General Purpose Solution - In Production Now

General purpose architecture suitable for shared memory processing and point-to-point communication

- 308 Lead CQFP, Hermetic
- 25 mil Pitch
- 2.05 in sq
- 0.160 in Height

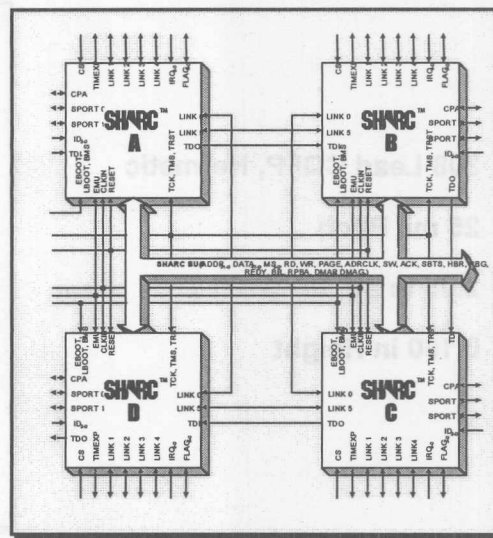




AD14160 General Purpose Solution - In Production Now

General purpose architecture suitable for shared memory processing and point-to-point communication

- 452 CBGA, Hermetic
- 1.85 in sq
- 0.200 in Height





AD14060

Electrical Performance Improvements

- **AD14060 Combines High-Performance Chip Design With High-Speed Interconnect Design for a Complete “Integrated Chip Solution”**
 - **Improved Multiprocessor Performance**
 - **Lowers Risk in Meeting TTM**
 - **Reduces System Test Burden**
 - **Improves Performance Density**

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AD14060

Electrical Performance Improvements (con't)

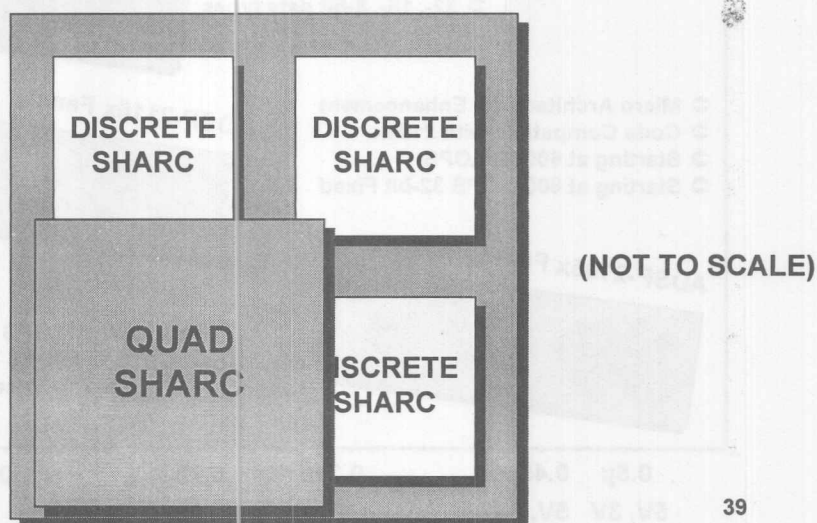
- **Minimized Crosstalk**
 - **Controlled Impedance**
 - **Every Trace Interactively Monitored in Routing**
 - **Parallelism Minimized**
- **Reduced Ground Bounce**
 - **Integral GND/PWR Planes**
 - **Optimized Low-Inductance Wirebonding**
- **Propagation Delays**
 - **Minimized in All Cases**
 - **Clock Traces Minimized and Matched**

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Board Size Reduction With Single Package DSP MCMs

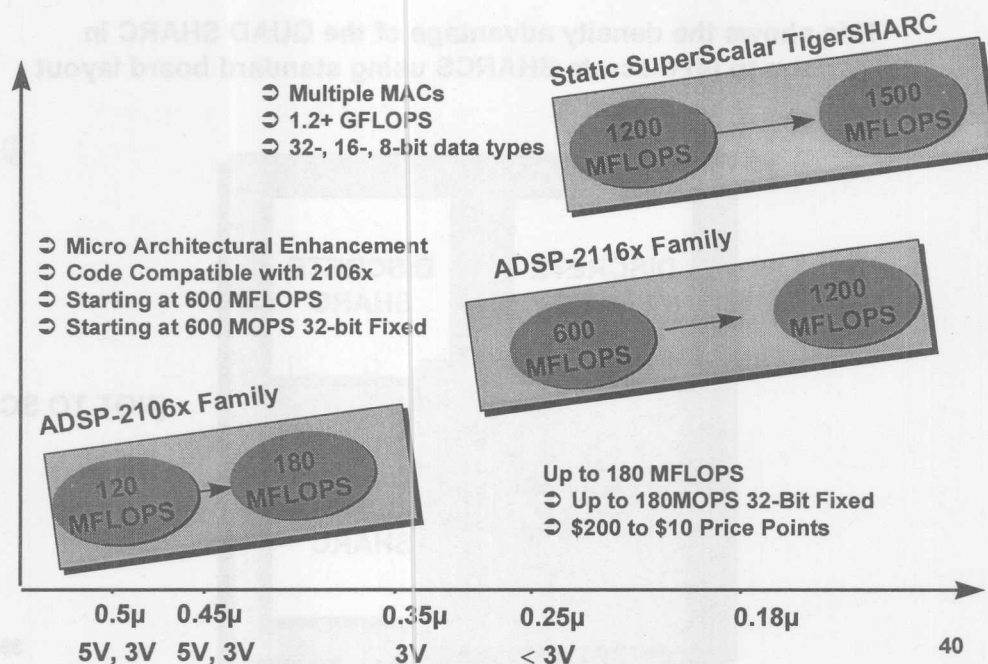
This shows the density advantage of the QUAD SHARC in
comparison to (4) discrete SHARCS using standard board layout



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32 Bit SHARC DSP Roadmap

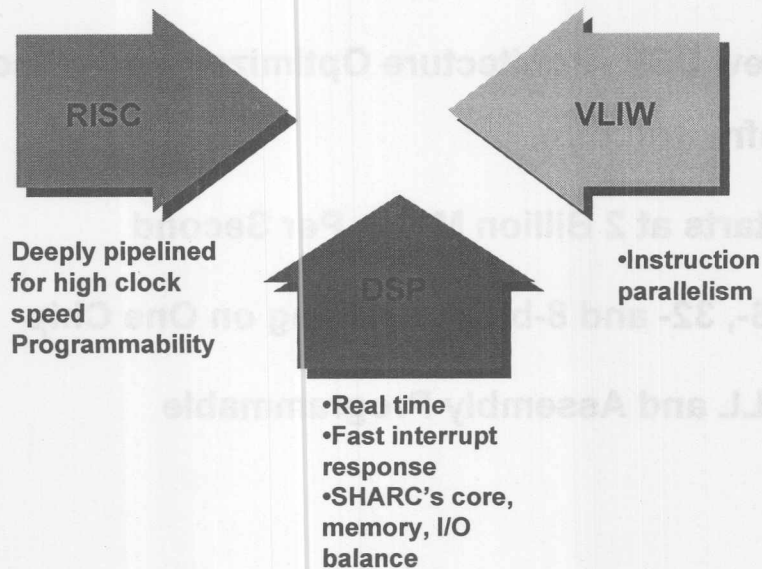




Introducing TigerSHARC™

- **New DSP Architecture Optimized for Telecom Infrastructure**
- **Starts at 2 Billion MACs Per Second**
- **16-, 32- and 8-bit Processing on One Chip**
- **HLL and Assembly Programmable**

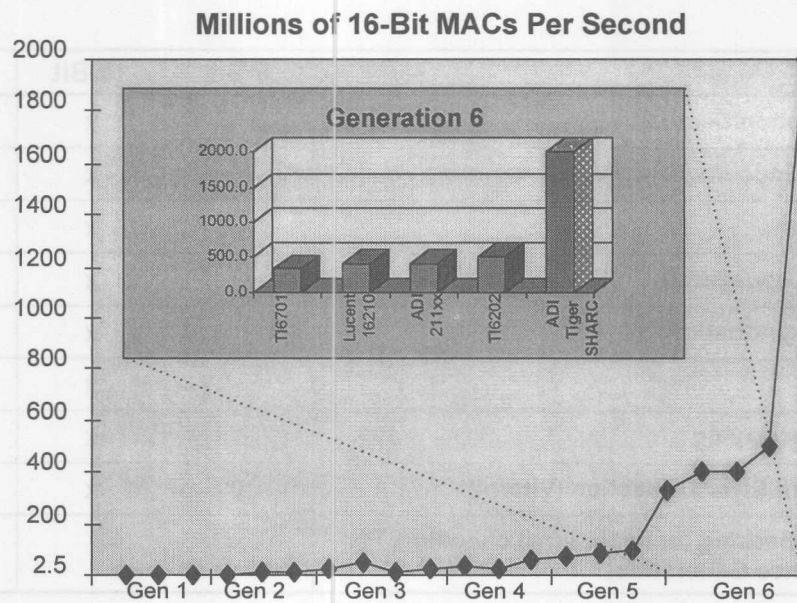
TigerSHARC™ Blends Architectural Approaches



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TigerSHARC™ : A New Level of Performance



Source: Forward Concepts

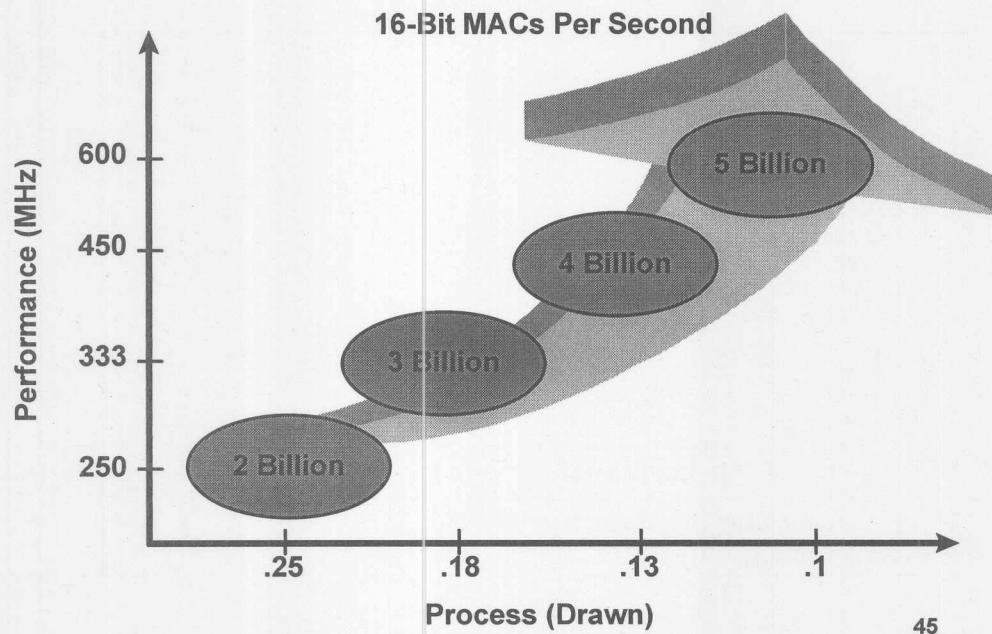


TigerSHARC™ Enables Precision & Performance Tuned to the Task

	8 Bit	16 Bit	32 Bit
Modulation/Demodulation		X	
Voice Encoding/Decoding		X	
Filtering		X	X
Echo Cancellation		X	X
Line Equalization		X	X
FFT		X	X
De-Interleaving		X	
Forward Error Correction (Viterbi)	X	X	
Bit Processing (convolutional encoding, PN Sequence Generation)	X		X



TigerSHARC™ : Platform for the Next Decade of Telecom Infrastructure Applications





TigerSHARC™: Platform for the Next Decade
of Telecom Infrastructure Applications





Embedded DSP Solutions

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Embedded DSP Solutions

**Embedded DSP Solutions utilize ADSP-21xx DSP
Cores Augmented with Application-specific Software
and/or logic to provide optimized solutions for:**

- **Remote Access Servers**
- **Secure Data Communications**
- **Embedded Speech Processing**



Remote Access Server Modems (RAS)



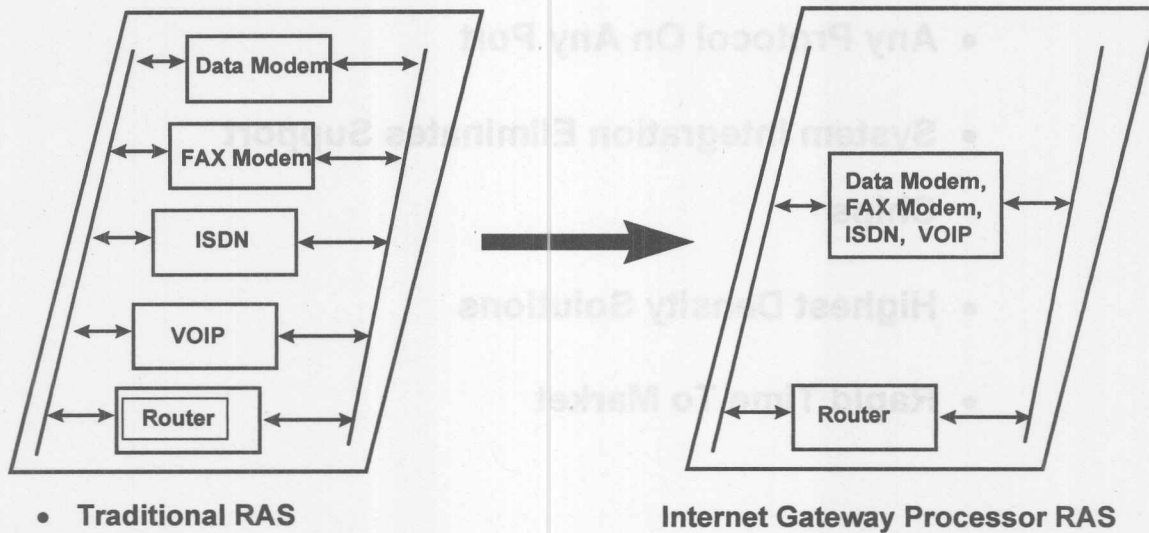
Internet Gateway Processors for RAS Applications

- **Any Protocol On Any Port**
 - **Flexible Architecture With Dedicated Resources Per Port**
- **Field Upgradable**
 - **RAM-Based Program Storage**
- **High Density of Ports**
 - **Memory and System Interfaces Integrated On-Chip**
- **Long Operating Life**
 - **Low Power Consumption and Minimal Cooling Required**
- **Programmable With Development Tools and SW Base**

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Four Processors In One



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Key Features of ADI Internet Gateway Processors

- Any Protocol On Any Port
- System Integration Eliminates Support Chips
- Highest Density Solutions
- Rapid Time To Market



ADSP-21mod970: Multiport Internet Gateway Processor



Enabling the World's Highest Density

- **Six Modems in a 1.45 sq. in. Space!**
- **3X More Density Than Any Other Solution**
- **Any Protocol On Any Port**

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ADSP-21mod970

Internet Gateway Processor

- **Supports Any Protocol On Any of the Six Ports**
- **Six V.34/56Kbps, HDLC, or FAX Modem Ports**
- **80 mW Typical Power Dissipation Per Port**
- **ADSP-21xx Code Compatible**
- **Designed For Flexible Processing**
 - **312 MIPS Processing Capacity**
 - **960 Kbytes On-Chip SRAM**



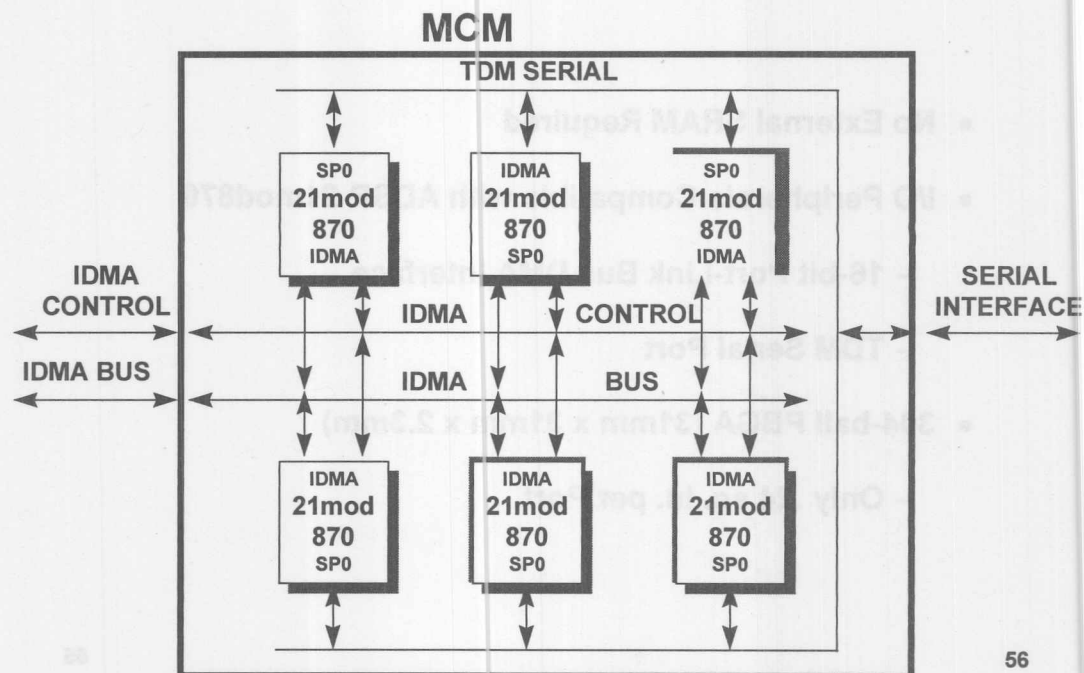
ADSP-21mod970 Internet Gateway Processor

- No External SRAM Required
- I/O Peripherals Compatible with ADSP-21mod870
 - 16-bit Port-Link Bus DMA Interface
 - TDM Serial Port
- 304-ball PBGA (31mm x 31mm x 2.3mm)
 - Only .24 sq. in. per Port

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ADSP-21mod970 Configuration





ADSP-21mod870 Key Features

- **Single Chip Modem Implementation**
- **V.34/56K and V.42/V.42bis controller code.**
- **52 MIPS Performance at 3.3V**
- **160K Bytes On-Chip SRAM**
- **16K x 24 PM plus two 8K x 24 overlay segments**
- **16K x 16 DM plus two 8K x 16 overlay segments**



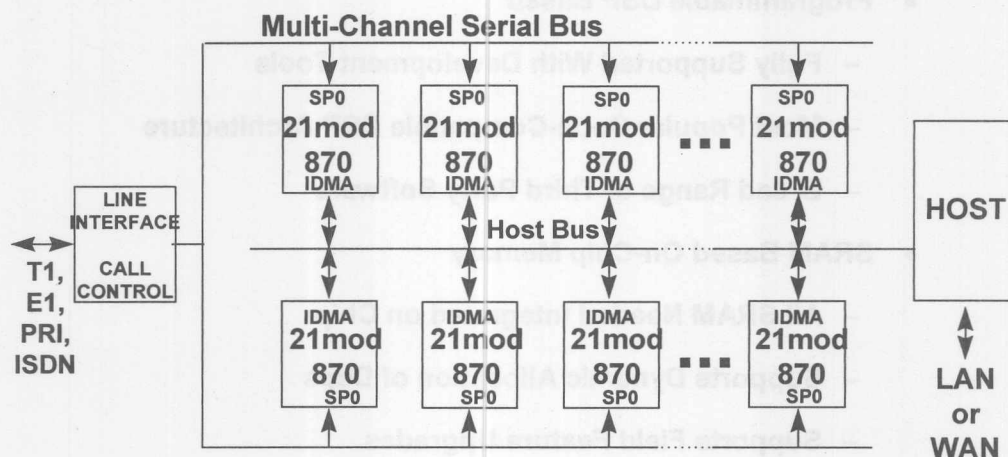
ADSP-21mod870 Key Features

- 16-bit DMA Port for host downloads
- TDM Serial port supports T1/E1
- Powerdown and low-power idle modes
- 100 lead TQFP package -- .4 square inch footprint
- Maximum Power = 140mW at 3.3V and 40MIPS
- Fully ADSP-21xx Code Compatible

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Network Access System



ADSP-21mod870 Functions

V.34 Modem	DTMF Dialing
56K Modem	PPP Framing
V.17 FAX	HDLC protocol
V.42, V.42bis, MNP2-5	

Host Functions

Multi-DSP Control, Data and Overlay Management



ADI Open Architecture

- **Programmable DSP Based**
 - **Fully Supported With Development Tools**
 - **Most Popular Code-Compatible DSP Architecture**
 - **Broad Range of Third Party Software**
- **SRAM Based On-Chip Memory**
 - **All SRAM Needed Integrated on Chip**
 - **Supports Dynamic Allocation of Dsp's**
 - **Supports Field Feature Upgrades**
- **Customizable**
 - **Object and Source Code Licenses**
 - **Utilize DSP Resources for Non-Modem Functions**

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RAS Modem Software Features

- **ISDN B-Channel HDLC**
- **Data Modulations**
 - **K56flex (30k-56k)**
 - **ITU-T V.34: 33600 bits/s - 2400 bits/s**
 - **CCITT V.32bis: 14400 bits/s - 7200 bits/s**
 - **CCITT V.32: 9600 bits/s - 4800 bits/s**
- **Start-up Procedures**
 - **ITU-T V.8**
- **CCITT V.42 Error Correction (LAPM & MNP 2-4)**
- **CCITT V.42bis data & MNP Class 5 Compression**
- **Software Interface API With Example Code**

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RAS Modern Software Features

- ISO 8-B-Channel HDLC
- Data Modulations
 - K56flex (10K-56K)
 - ITU-T V.34: 3300 bits - 14400 bits
 - CCITT V.32bis: 14400 bits - 17200 bits
 - CCITT V.32: 9600 bits - 4800 bits
- Start-up Procedures
 - ITU-T V.8
 - CCITT V.42 Error Correction (LAPM & MNP 2-4)
 - CCITT V.42bis data & MNP Class 5 Compression
 - Software Interface API With Example Code

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Embedded Speech Processing (ESP)



Hands Free Car Kits Speech Processing Application

Programmable
DSP Technology enables--



- The Clearest, Most Intelligible Speech Quality
- Concurrent Talk AND Listen Capability
- Speech Recognition for Voice Activated Commands and Dialing
- Swift Addition of Value-Added Software Features

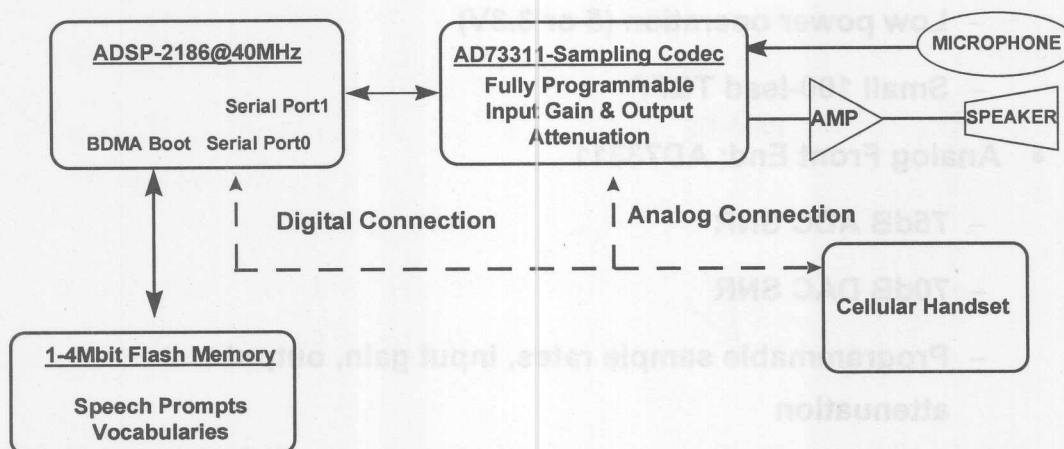
A DEVICE DESIGNED TO ENABLE SAFE CELLULAR COMMUNICATIONS WHILE DRIVING IN AN AUTOMOBILE!!!

64



Full-Duplex Hands-Free Car Kit

The ADSP-21xx architecture enables efficient execution of HF&SR algorithms while minimizing system components and interconnect.



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Embedded Speech Processing Chipset

- **Low Cost 16-Bit Programmable DSP: ADSP-2186/2184**
 - 40K/20K Bytes on-chip SRAM
 - Low power operation (5 or 3.3V)
 - Small 100-lead TQFP
- **Analog Front End: AD73311**
 - 75dB ADC SNR
 - 70dB DAC SNR
 - Programmable sample rates, input gain, output attenuation

66

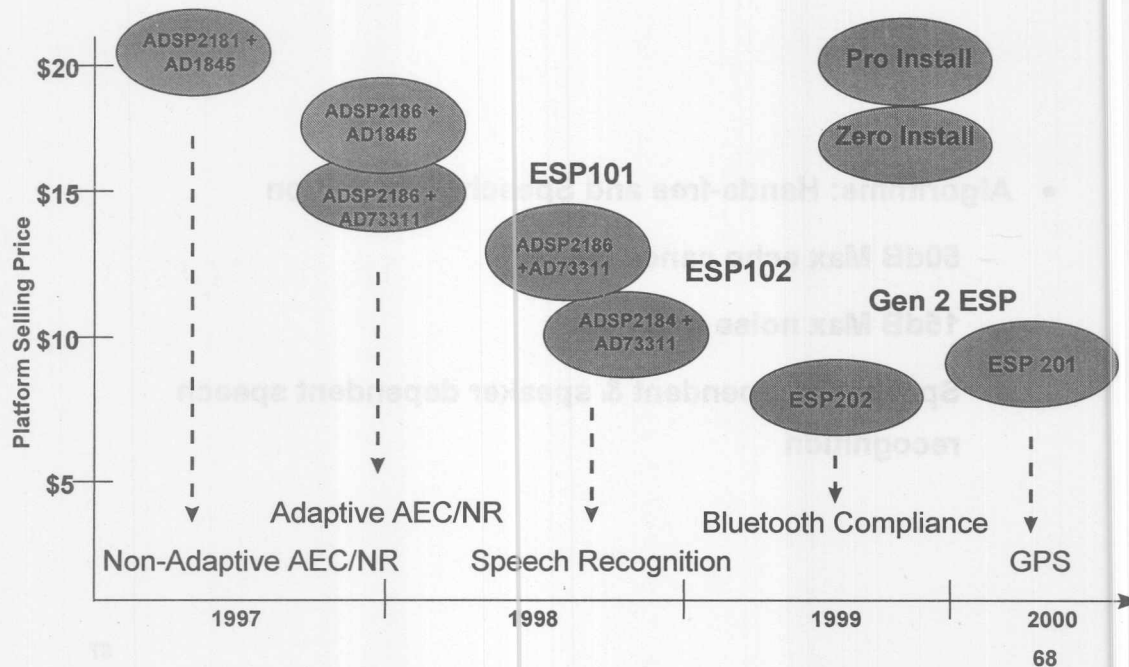


Embedded Speech Processing Chipset

- **Algorithms: Hands-free and Speech Recognition**
 - **50dB Max echo cancellation**
 - **15dB Max noise reduction**
 - **Speaker independent & speaker dependent speech recognition**



ESP Roadmap Offers a Code Compatible, Mixed Signal Migration Path





Secure Data Communications



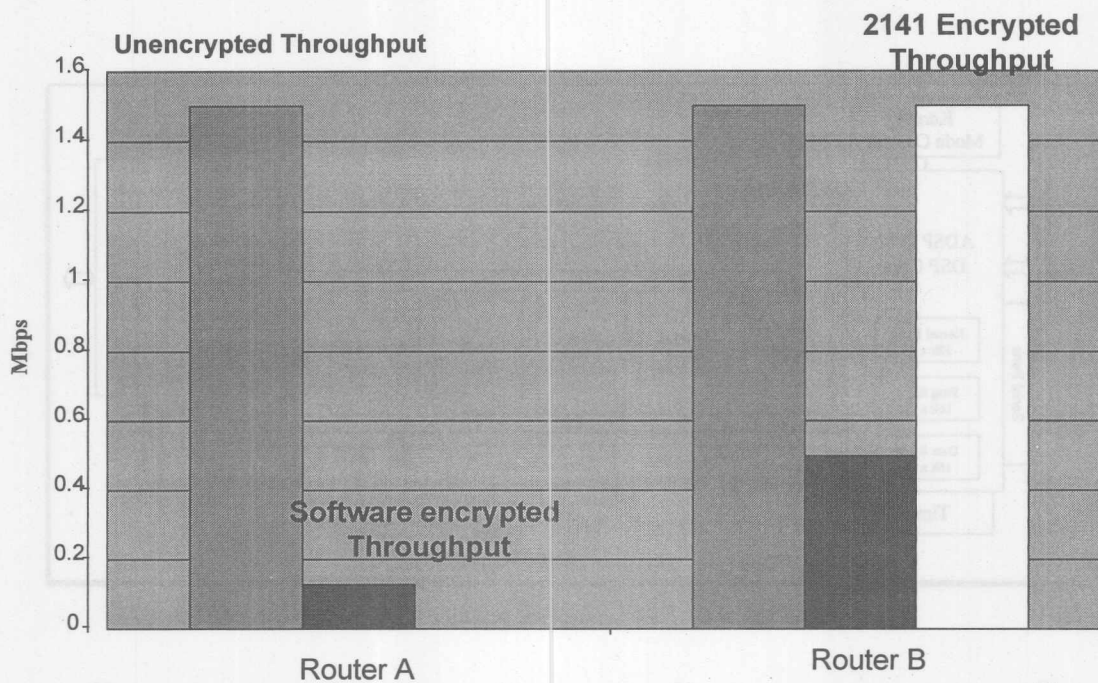
What is Secure Data?

- **Providing Encryption, Authentication and Certification of Data Communications**
- **For Example: Enabling Corporations to Create a VPNS (Virtual Private Networks) Over Public Networks While Lowering Their Costs and Increasing the QOS (Quality of Service) of Their Systems**
- **Security Functions May Be Provided in Software; Hardware Is Used Where High Throughput Is Required--for Example in High and Mid-Range Routers**

70



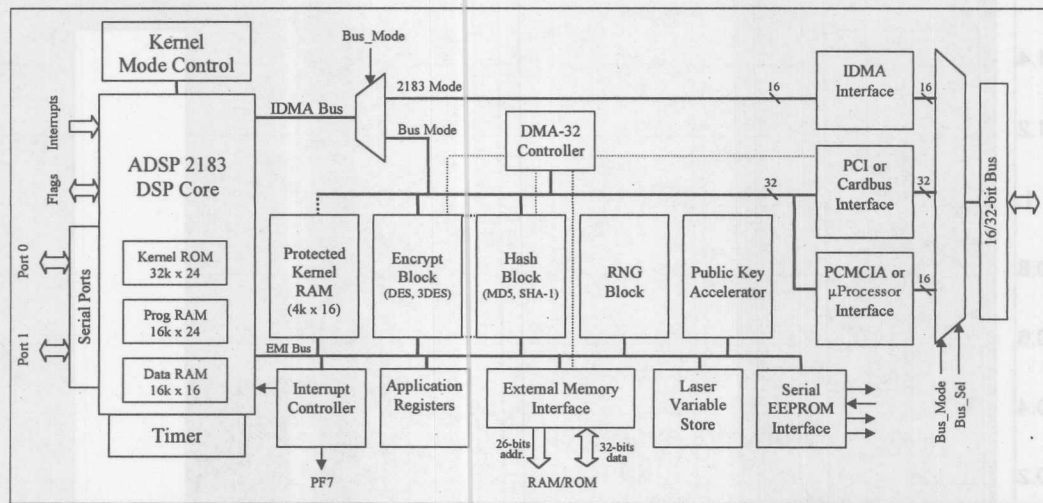
The ADSP-2141 Difference



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SafeNet ADSP-2141 Block Diagram



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ADSP-2141 Performance Characteristics

- **Highest Hash/encryption throughput in the industry**
 - **DES at 640 Mbps**
 - **3-DES at 214 Mbps**
 - **MD5 at 315 Mbps**
 - **SHA-1 at 253 Mbps**
- **On chip acceleration of Public Key Interface (PKI), including non-deterministic Random Number Generation**
- **One-pass IPSEC transforms with target IPSEC, TDES throughput of OC-3 (155 Mbit/s)**



ADSP-2141 Performance Characteristics

- Highest Hash/Encryption throughput in the industry
 - DES at 640 Mbps
 - 3-DES at 214 Mbps
 - MD5 at 315 Mbps
 - SHA-1 at 253 Mbps
- On-chip acceleration of Public Key Interface (PKI), including non-deterministic Random Number Generation
- One-pass 198EC transforms with target 198EC, TDES throughput of 0.3 (186 Mbps)

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DSP Tools from ADI & Partners



DSP Tools from ADI & Partners



VisualDSP: A Common Platform for DSP Development

- **VisualDSP Will Be a Common Platform for Development Across All Analog Devices DSP Families.**
- **VisualDSP 2.0 Contains**
 - **Debugger Front-End**
 - **Integrated Development Environment**
- **VisualDSP Will First Support the SHARC Family, and Will Be Bundled With the Next Release of SHARC Tools, 4.0.**

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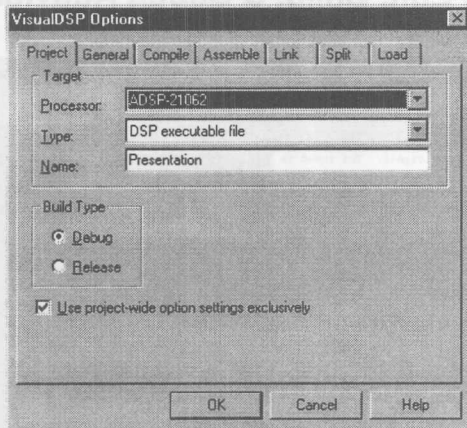


What is an Integrated Development Environment?

- **One Windows Application That Controls All the Functions Needed to Generate Code.**
 - File Editing
 - Tool, File and Build Management
 - Control of Assembler, Compiler, Linker, Loader and Splitter
 - Help and Error Indexing
- **Common Environment and Published APIs Enable Third Party Tools to Operate in VisualDSP IDE.**

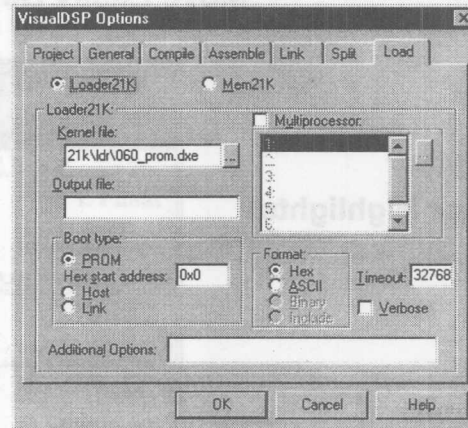


Setup Projects & Specify Tool Options via Dialog Boxes



**Set Project Wide
or Individual Settings**

**Create Debug or Release
Mode Builds**



**Easily Configure & Modify
Tool Options**

**Don't need to Learn Command
Line Syntax**

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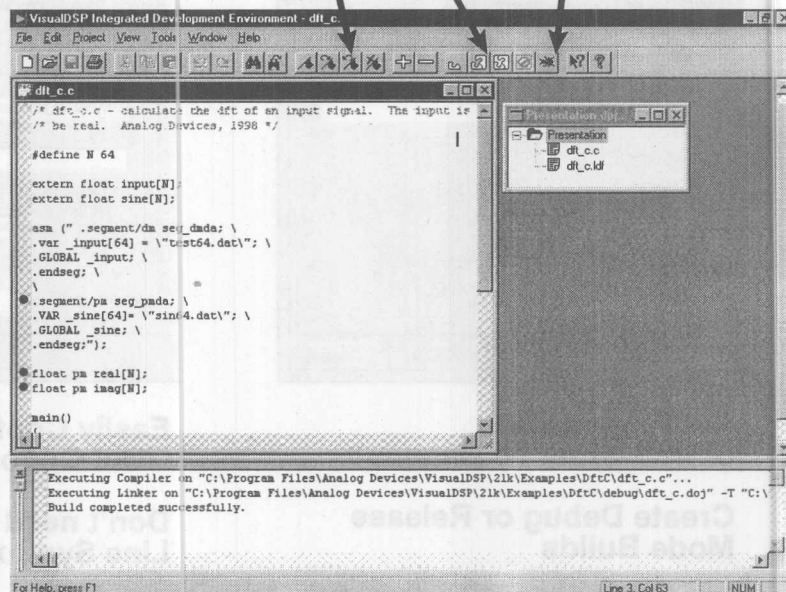
Flexible Project Management & Editing

Move Easily Between Edit, Build, & Debug Activities

Editor Highlights
ADI Syntax

Insert
Bookmarks

View Build
Results





VisualDSP Debugger Session

Profile code to
Identify Bottlenecks

Create Custom
Register Windows

View Mixed C and
Assembly Listings

Profile

Start Addr	End Addr	Memory	Exec %	Exec Cycles	Exec Count	Read Count	Write Count
_main	zero_pm	Program...	100.000...	197783	164880	156824	0
0x20119	0x20141	Program...	99.9615...	197707	164805	156747	0
0x2011d	0x2013c	Program...	58.4093...	115525	99009	94917	0
0x2011d	0x20127	Program...	6.60263...	13059	12329	12868	0

Cache An...

```

CL 00000000
CH 00000000
R1 3EC3EF1500
R3 0000000000
M12 00003F
  
```

Disassembly

```

finish_inits
[000201CC] rts;
[000201CD] call (pc, 0xffffffff9a);
[000201CE] call (pc, 0xffffffff96);
[000201CF] rts (db);
[000201D0] m14=0x1;
[000201D1] l12=0;
_exit
[000201D2] r5=r5-r5, l4=m13;
[000201D3] i4=0x28124;
[000201D4] r2=pass r4, r0=dm(i4,m6);
  
```

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VisualDSP 2.0 / SHARC 4.0 Release

- **VisualDSP Debugger & Integrated Development Environment**
- **Supports ADSP-21060, -21061, -21062, and new -21065L**
- **Operates on Windows NT and Windows 95**
- **New C Compiler**
- **New Linker Technology**
- **On-line Documentation**
- **Released**

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New SHARC C Compiler (Included in VisualDSP 2.0)

- **New Optimizing C Compiler for 2106X**
 - Not GNU based
 - Edison Design Group/Kuck and Assoc. Front End
 - Edinburgh Portable Compilers code generator
- **Extensions to ANSI C**
 - dm/pm, inline assembly, numerical, complex
- **Integrated into IDE**



16 Bit Family Software Tools Release 6.0

- **Released**
- **2100 Family Software Tools Release 6.0 Includes**
 - **VisualDSP Debugger for Simulator**
 - **New Linker with Overlay Support**
 - **Bug Fixes on Assembler, Compiler, Loader, Splitter**
- **Supports Windows 95 and Windows NT**

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ADSP-218x EZ-ICE Software Release 2.0

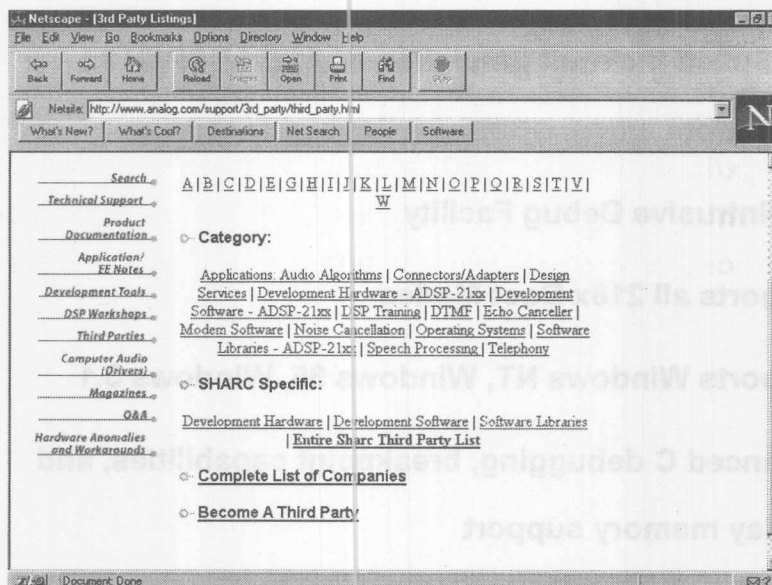
- **Released**
- **Full-Speed Incircuit Emulation of *ALL* ADSP-218x Processors**
- **Non-Intrusive Debug Facility**
- **Supports all 218x Boot Modes**
- **Supports Windows NT, Windows 95, Windows 3.1**
- **Enhanced C debugging, breakpoint capabilities, and overlay memory support**

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ADI Third Party Web Site. Bookmark It!

www.analog.com/support/3rd_party/third_party.html



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Web Third Party Developers Directory

- **Alphabetical Listing**
- **Categories**
 - **Audio Algorithms/Connectors/Adapters/Design Services/Development Hardware ADSP-21xx/Development Software ADSP-21xx/DSP Training/DTMF/Echo Canceller/Modem Software/Noise Cancellation/Operating Systems/Software Libraries-ADSP-21xx/Speech Processing/Telephony**
- **SHARC Specific**
 - **Development Hardware**
 - **Development Software**
 - **Libraries**

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Web Third Party Developers Directory

- Alphabetical Listing
- Categories
 - Audio Algorithm/Connector/Adapter/Design
 - Services/Development Hardware ADSP-
 - 21xx/Development Software ADSP-21xx/ADSP
 - Training/DSP/Echo Cancellation/Software/Noise
 - Cancellation/Operating Systems/Software Libraries-
 - ADSP-21xx/Speech Processing/Telephony
- SHARC Specific
 - Development Hardware
 - Development Software
 - Libraries

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Systems and Solutions from Analog Devices



Systems and Solutions From Analog Devices

ADI's Software & Systems Technologies Division is dedicated to providing the building blocks for OEM Solutions

- **Algorithm Chipsets Available Using ADI Silicon Products and Globally Sourced Software Object Code Modules**
- **Reference Designs Available, Including Orcad Files, Documentation, Software, Bill of Materials**
- **"Black Box" Type Modules for Fast Time to Market in Engineering Challenged Environments:**
 - **Digital Telephony (Low End and High End Featurephones)**
 - **High Quality Audio (Dolby Digital, DTS, THX, MPEG)**
- **Flexible Engineering Business Models Designed to Add Value and Add Expertise to OEM Engineering Challenges**

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Algorithm Building Blocks available on ADI DSPs

V.34	V.17	V.34 bis	V.42	V.32
Dolby AC-3	MPEG I Decode	MPEG I Encode	GPS Soft Navigator	GPS Soft Correlator
JPEG	DECT	GPS RF Front End	Acoustic Echo Cancellation	
G.728	G.723.1	G.722	G.165	G.729
H.323	H.320	MPEG II Encode	MPEG II Decode	THX
DTS	MPEG Video	H.324	Hi Quality Audio	Energy Meters
6.6 MGSM	4.8 CELP	Caller ID	Speaker-phone	Noise Cancellation
ISDN	Video Encode	Video Decode	AEC	

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Audio Algorithms for the SHARC Product Line

- **Dolby Digital (AC-3) multichannel decode**
- **Dolby Pro-Logic Decode**
- **MPEG-II Decode Layer I and Layer II**
 - complies with ISO/IEC 13818-3 audio standard
 - MPEG Audio I / II also available on ADSP-218X product
- **THX Home Theater Decode**
- **DTS Multi-channel Decode (Expected Release Date: May 1998)**

***Evaluation board available,
contact ADI Systems & Solutions Division Hotline:
systems.solutions@analog.com***

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Telephony Algorithms

- Acoustic Echo Cancellation
- Tone generation, DTMF
- DTMF receiver
- Call Progress Tone detection
- Caller ID
- Caller ID on Call Waiting
- AGC
- Voice Activity Detector
- Fax CNG Detection
- MGSM Speech Compression (note, that other speech compression algorithms are also available, such as CELP and G.723)
- V.34 Fax Modem (56K in development)

*Available as object code
modules, or with DSP
Kernel for Featurephone*

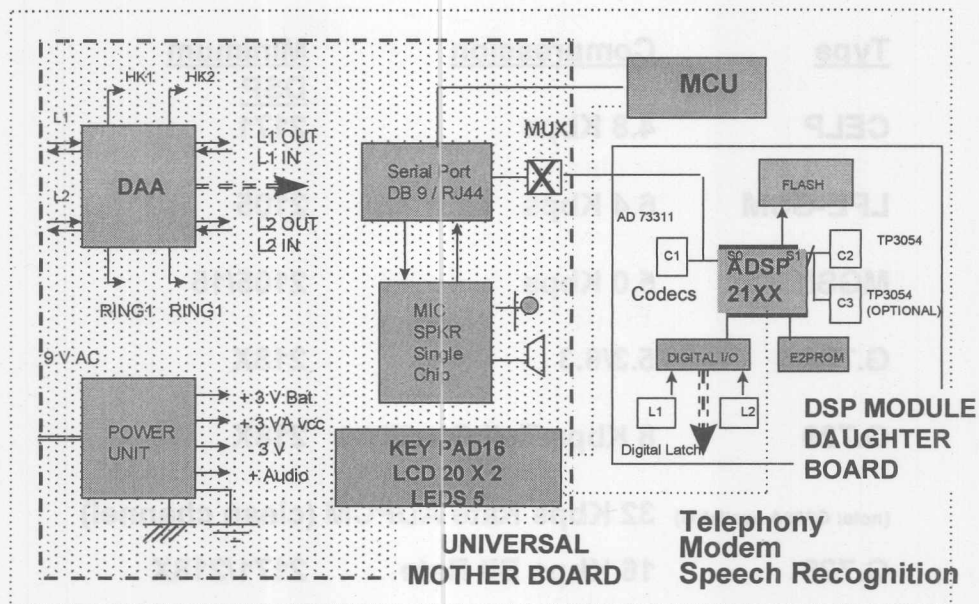


Telephony/Modem Algorithms

- **Full Duplex Speakerphone**
 - Includes Caller ID Type I and II, DTMF and Call Progress
 - AEC (G.167), LEC (G.165), And Automatic Gain Control
- **Digital Answering Machine**
 - 5.0Kbps Modified GSM Speech Compression for 15 Minutes of
Stored Voice
- **V.34 Modem (56K Available Summer 1998)**



Digital Telephony Platform



Suitable for Low end / High End Featurephones

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Compression Algorithms

<u>Type</u>	<u>Compression</u>	<u>Minimum DSP</u>
CELP	4.8 Kbps	2171
LPE-GSM	6.4 Kbps	2105
MGSM	5.0 Kbps	2105/15
G.723.1	5.3/6.3	218X
G.729	8 Kbps Toll Quality	218X
(note: G729A available)	32 Kbps Rate ADPCM (clean channel)	
G.728	16 Kbps Bit Rate	2171/218X

Available as object code modules, or with DSP Kernel for Featurephones



H.324 Videophone

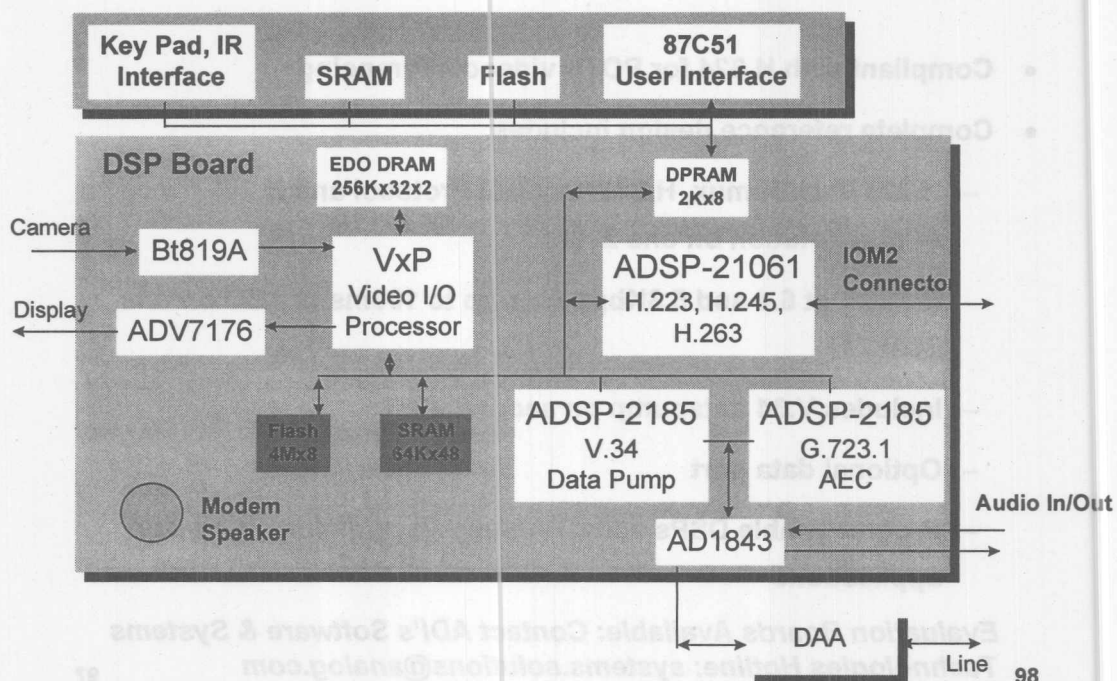
- Compliant with H.324 for POTS videoconferencing
- Complete reference design includes:
 - H.223 Mux/Demux, H.245 Control Protocol and H.263 for up to 4CIF resolution on one 21061
 - G.723.1 at 6.4 and 5.3Kbps plus up to 100ms of AEC on one 2181
 - Includes V.34 datapump on second 2181
 - Optional data port
 - Programmable DSPs allow for support of multimedia audio applications

Evaluation Boards Available: Contact ADI's Software & Systems Technologies Hotline: systems.solutions@analog.com

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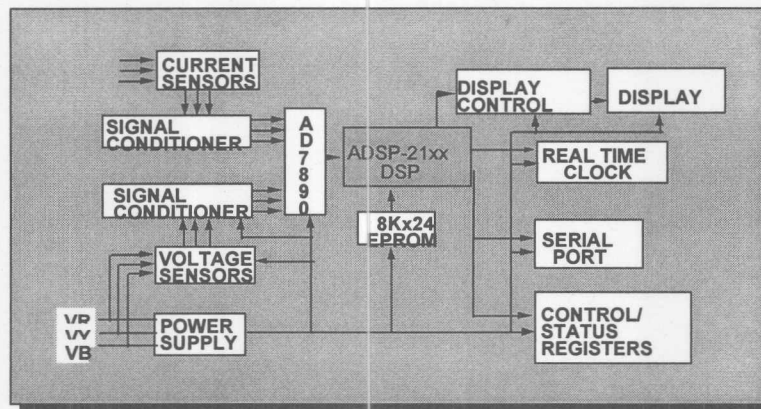


H.324 Videophone - Rev. 2

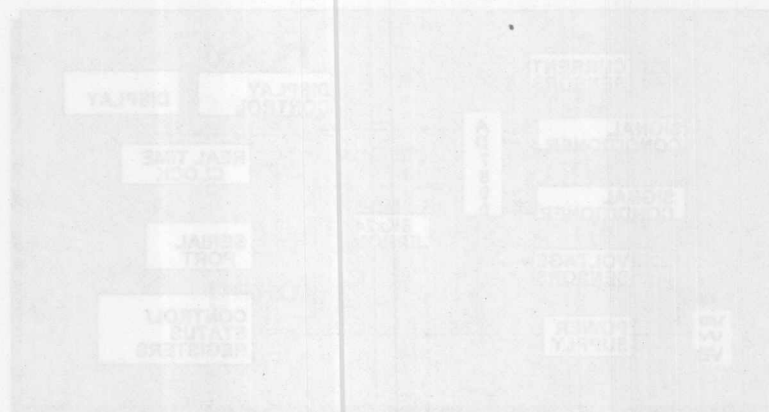




Salem 3-Phase Energy Meter



- 3-Phase, 3-Wire/4-Wire Supply
- 0.5% Accuracy
- Multiple Programmable Measurements



- 3-Phase 3-Wire Supply
- 0.5% Accuracy
- Multiple Programmable Measurements



SECTION 6

DATA CONVERTER SUPPORT COMPONENTS

Low Power, Low Drop Out Voltage References

High Speed, Buffered Video Muxes

High Speed Crosspoint Switches

CMOS Switches and Multiplexers



SECTION 6 DATA CONVERTER SUPPORT COMPONENTS

Low Power, Low Drop Out Voltage References

High Speed, Buffered Video Muxes

High Speed Crosspoint Switches

CMOS Switches and Multiplexers



Voltage References



The ADR2X Series...
A Revolutionary New Family of
Precision, Micropower
Voltage References That Employ a Unique
XFET™ Architecture to Achieve Very
Low Noise and Very Low Power
Consumption!



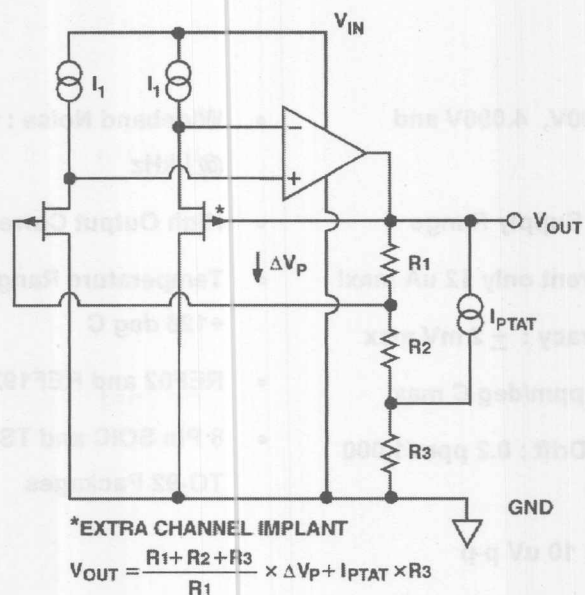
ADR290, ADR291 ADR292 and AD2R93 Micropower Precision References

- 2.048V, 2.500V, 4.096V and 5.000V
- 2.7V to 15V Supply Range
- Supply Current only 12 uA max!
- Initial Accuracy : ± 2 mV max
- Tempco : 5 ppm/deg C max
- Long Term Drift : 0.2 ppm/1,000 hours
- Low Noise : 10 uV p-p
- Wideband Noise : 95 nV/ root Hz @ 1 kHz
- High Output Current : 5 mA min
- Temperature Range : -40 deg C to +125 deg C
- REF02 and REF19X Pinout
- 8 Pin SOIC and TSSOP and 3 lead TO-92 Packages

6-5



XFET™ Simplified Block Diagram



6-6



ADR2X Family

- **XFET Design Offers Lower Noise Than Conventional Bandgap References**
- **ADR2XX Operating at 12 μ A Exhibit the Same Noise As Bandgaps Operating at $> 100 \mu$ A**
- **Wide Operating Temperature Range (-40 deg C to +125 deg C) Makes the ADR2X Suitable for Use in Automotive, Communications and Instrumentation Applications**
- **Standard Ref-02 and Ref19X Pinout Allows for Future Upgrade**

6-7



ADRX Family

- XFET Design Offers Lower Noise Than Conventional Bandgap References
- ADRX Operating at 12 μ A Exhibits the Same Noise As Bandgap Operating at $> 100 \mu$ A
- Wide Operating Temperature Range (-40 deg C to +125 deg C) Makes the ADRX Suitable for Use in Automotive, Communications and Instrumentation Applications
- Standard Ref-02 and Ref-0X Pinout Allows for Future Upgrade

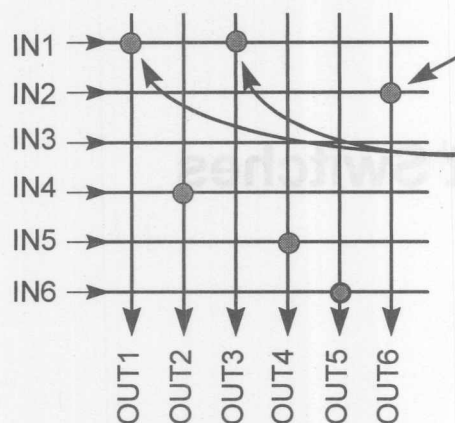


Video Crosspoint Switches



What's a Crosspoint Switch?

Example: 6 x 6 Switch



When this switch cell is activated, it connects IN2 to OUT6

"Non-Blocking" - Any output can access any input. (Even if another output is connected to that input)

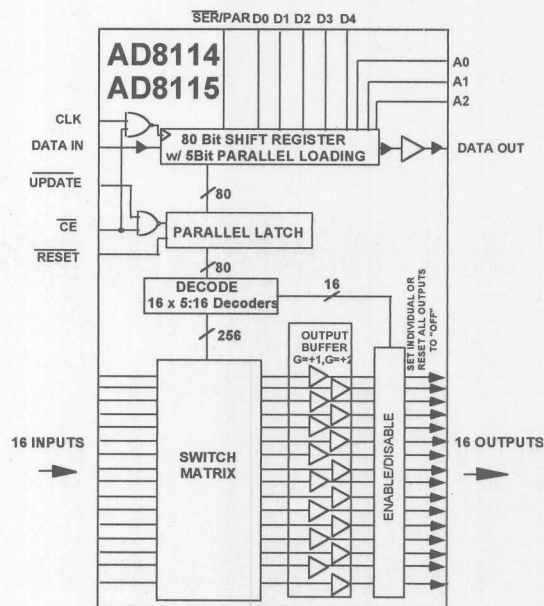
Example Switch Configuration

IN1 → OUT1 & OUT3
 IN2 → OUT6
 IN3 → N/C
 IN4 → OUT2
 IN5 → OUT4
 IN6 → OUT5



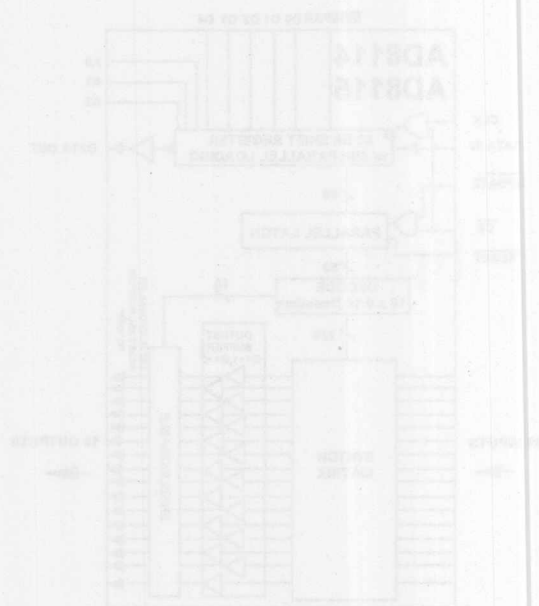
AD8114 and AD8115 16 x 16 Video Crosspoint Switches

- $G=+1$ (AD8114) & $G=+2$ (AD8115)
- High Speed : 300 MHz (-3dB)
- 400V/ μ s Slew Rate
- 0.05 dB Gain Flatness to 50 MHz
- 0.05%/0.05° Diff Gain/ Diff Phase Error ($R_L=150\Omega$)
- -72 dB Crosstalk @ 5 MHz
- -90 dB Off Isolation @ 10 MHz
- $\pm 5V$ Supplies @ 80 mA
- 100 pin TQFP Package





AD8114 and AD8115 16 x 16 Video Crosspoint Switches



- Q=1 (AD8114) & Q=2 (AD8115)
- High Speed : 300 MHz (-3dB)
- 400V_{pp} Slew Rate
- 0.05 dB Gain Flatness to 50 MHz
- 0.05% 0.05° DUT Gain, DUT Phase
- Error (R=150)
- -75 dB Crosstalk @ 5 MHz
- -80 dB Off Isolation @ 10 MHz
- $\pm 5V$ Supplies @ 80 mA
- 100 pin TQFP Package

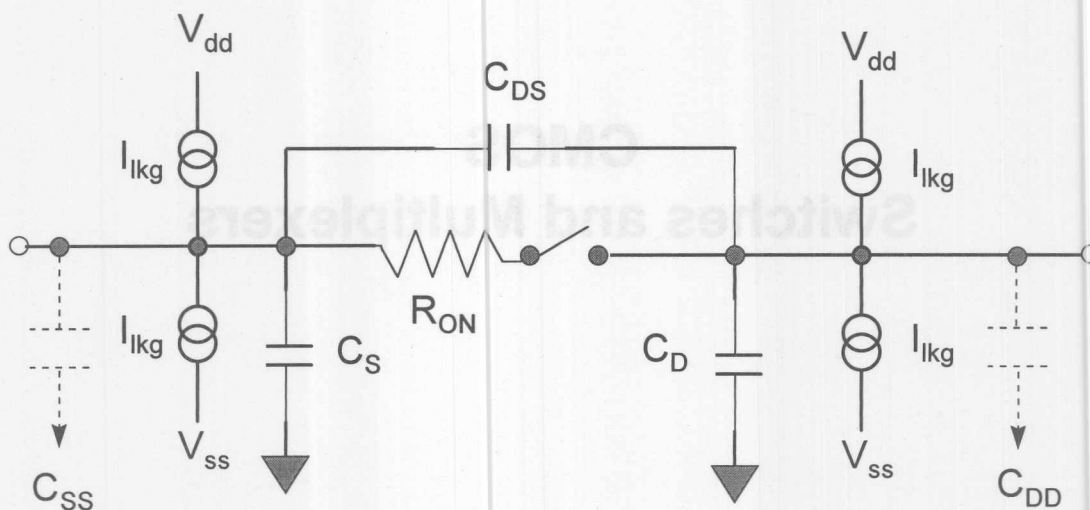
6-12



CMOS Switches and Multiplexers



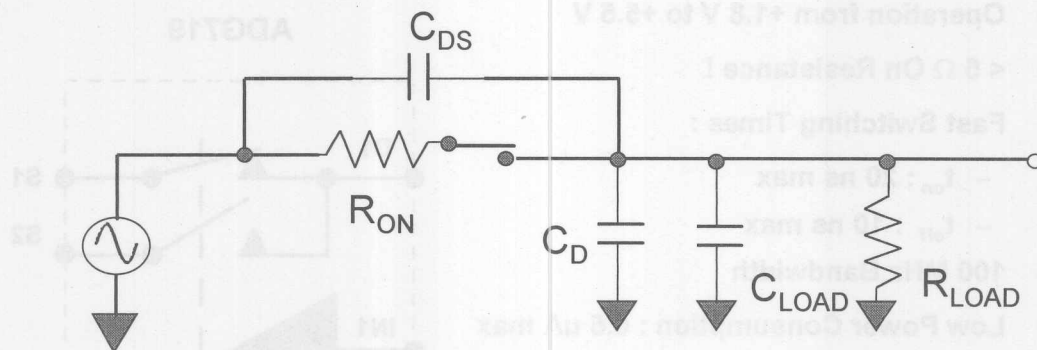
Important CMOS Switch Parameters...



6-14



Bandwidth Analysis



$$F_C = \frac{1}{(2\pi RC)}$$

$$R = \frac{R_L \times R_{ON}}{R_L + R_{ON}}$$

$$C = C_D + C_L$$

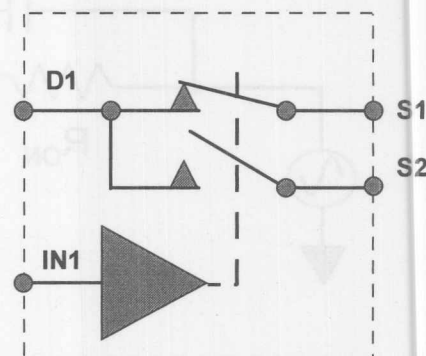
6 - 15



ADG719, ADG736 Single, Dual CMOS SPDT Switches

- Operation from +1.8 V to +5.5 V
- $< 5 \Omega$ On Resistance !
- Fast Switching Times :
 - t_{on} : 20 ns max
 - t_{off} : 10 ns max
- 100 MHz Bandwidth
- Low Power Consumption : 0.5 μ A max
- TTL/CMOS Compatible
- 6 Lead SOT-23 and 8-lead μ SOIC Packages (ADG719)
- 10 Lead μ SOIC Package (ADG736)

ADG719



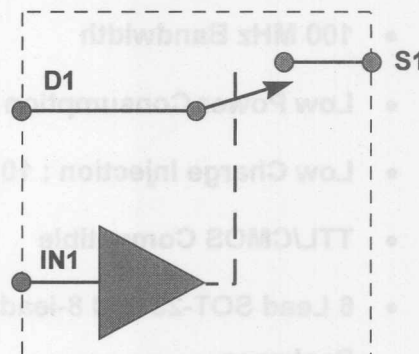
Switches Shown for Logic "1" Input

6-16



ADG701 and ADG702 Low R_{ON} Precision CMOS SPST Switches

- Operation from +1.8 V to +5.5 V
- 1 Ω Typical On Resistance !
- R_{ON} Flatness vs V_s : 1 Ω max
- Fast Switching Times
 - t_{on} : 20 ns max
 - t_{off} : 10 ns max



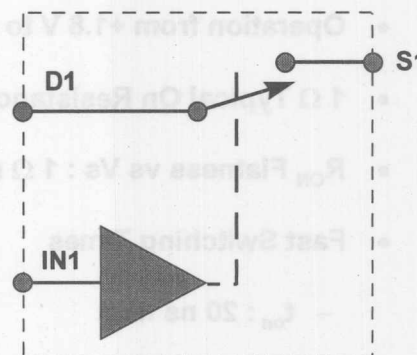
ADG701 : Normally Closed
ADG702 : Normally Open

6-17



ADG701 and ADG702 (con't)

- 100 MHz Bandwidth
- Low Power Consumption : 0.5 μ A max
- Low Charge Injection : 10 pC typ
- TTL/CMOS Compatible
- 6 Lead SOT-23 and 8-lead μ SOIC Packages



ADG701 : Normally Closed
ADG702 : Normally Open

6-18

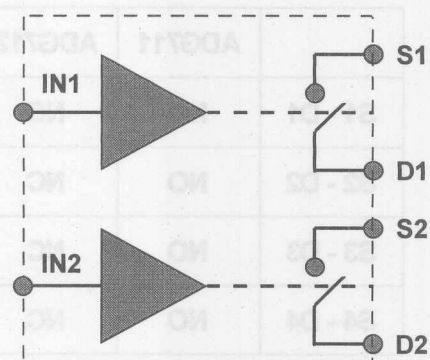


ADG721, ADG722 and ADG723 Dual CMOS SPST Switches

Dual Versions of the ADG701, ADG702

	S1 - D1	S2 - D2
ADG721	NO	NO
ADG722	NC	NC
ADG723	NO	NC

Switches Shown for a Logic "0" Input



8 Lead μ SOIC Package

6-19



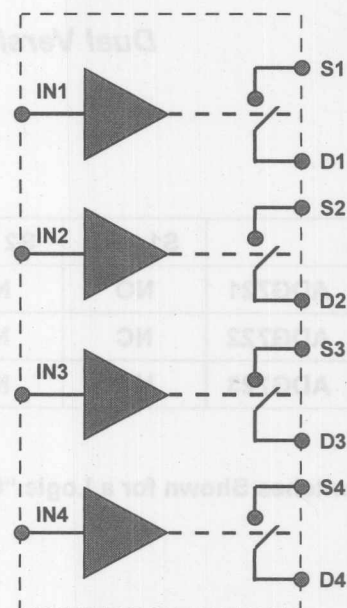
ADG711, ADG712 and ADG713 Quad CMOS SPST Switches

Quad Versions of the ADG701, ADG702

	ADG711	ADG712	ADG713
S1 - D1	NO	NC	NC
S2 - D2	NO	NC	NO
S3 - D3	NO	NC	NO
S4 - D4	NO	NC	NC

Switches Shown for a Logic "1" Input

16 Lead TSSOP Package



6-20

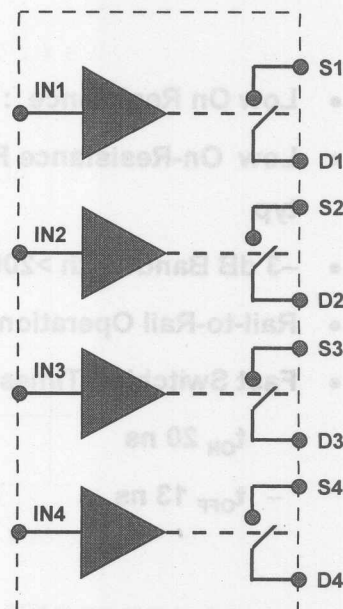


ADG661, ADG662, ADG663 Quad SPST Switches

- + 5V, \pm 5V Supply Operation
- On Resistance < 50 Ω
- 16 Lead TSSOP Package

	ADG661	ADG662	ADG663
S1 - D1	NO	NC	NO
S2 - D2	NO	NC	NO
S3 - D3	NO	NC	NC
S4 - D4	NO	NC	NC

Switches Shown for a Logic "0" Input

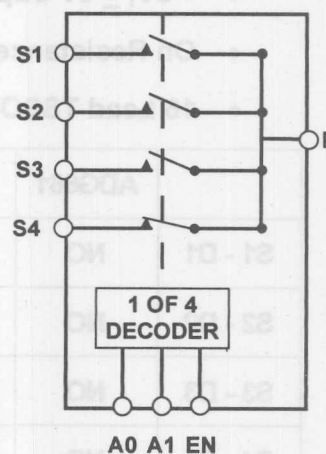


6 - 21



ADG704 4 Channel Multiplexer

- Low On Resistance : 2.5 ohm typ
- Low On-Resistance Flatness : 0.75 ohm, typ
- -3 dB Bandwidth >200 MHz
- Rail-to-Rail Operation
- Fast Switching Times :
 - t_{ON} 20 ns
 - t_{OFF} 13 ns

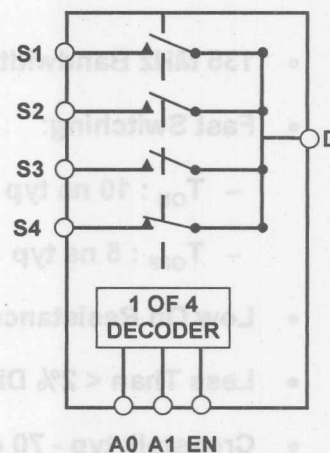


6-22



ADG704

- TTL/CMOS Compatible
- +1.8 V to +5.5 V Single Supply
- Typical Power Consumption (<0.01 mW)
- 10-Lead uSOIC Package

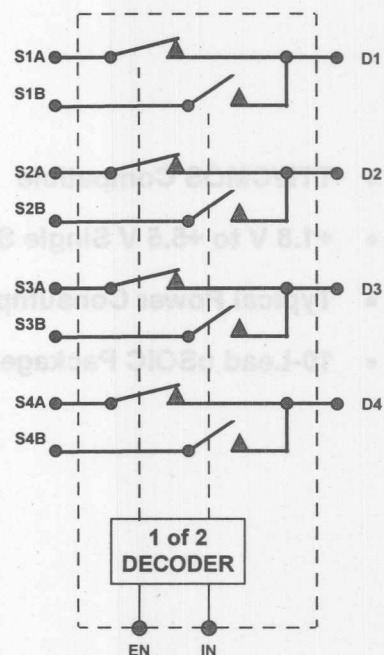


6-23



ADG774 Quad 2:1 Multiplexer

- 135 MHz Bandwidth
- Fast Switching:
 - T_{ON} : 10 ns typ
 - T_{OFF} : 5 ns typ
- Low On Resistance : 6 Ω typ
- Less Than < 2% Distortion
- Crosstalk typ - 70 dB @ 30 MHz

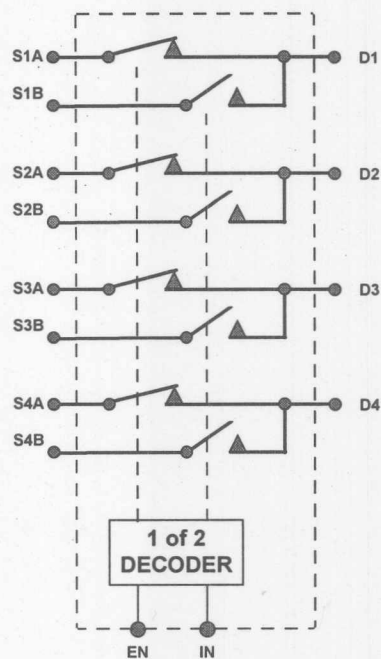


6 - 24



ADG774 (con't)

- Three State Outputs
- Single 3.3V/5V Operation
- 100 nA typ Quiescent Current
- Pin Compatible with P15L200



6 - 25



ADG774 (cont.)



- Three State Outputs
- Single 3.3V_{SW} Operation
- 100 nA typ Quiescent Current
- Pin Compatible with P16L300



SECTION 7

COMPUTER INTERFACE PRODUCTS

- **Electromagnetic Compatibility (EMC)**
- **European EMC Requirements**
- **RS-232 Line Driver/Receivers**
- **RS-485 Transceivers**
- **V.35 Transceiver**
- **Digital Isolators**



SECTION 7 COMPUTER INTERFACE PRODUCTS

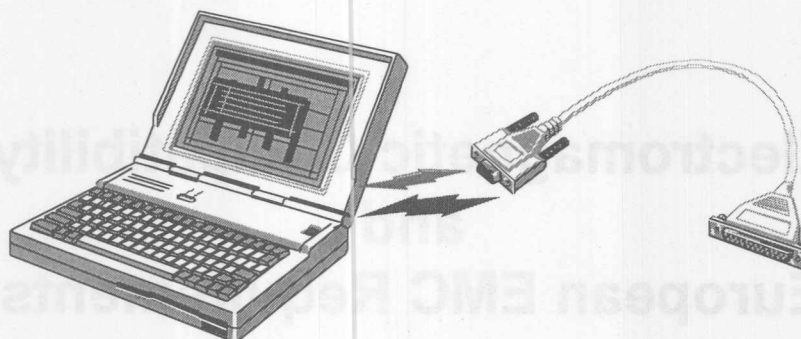
- Electromagnetic Compatibility (EMC)
- European EMC Requirements
- RS-232 Line Driver/Receivers
- RS-485 Transceivers
- V.35 Transceiver
- Digital Isolators



Electromagnetic Compatibility and European EMC Requirements



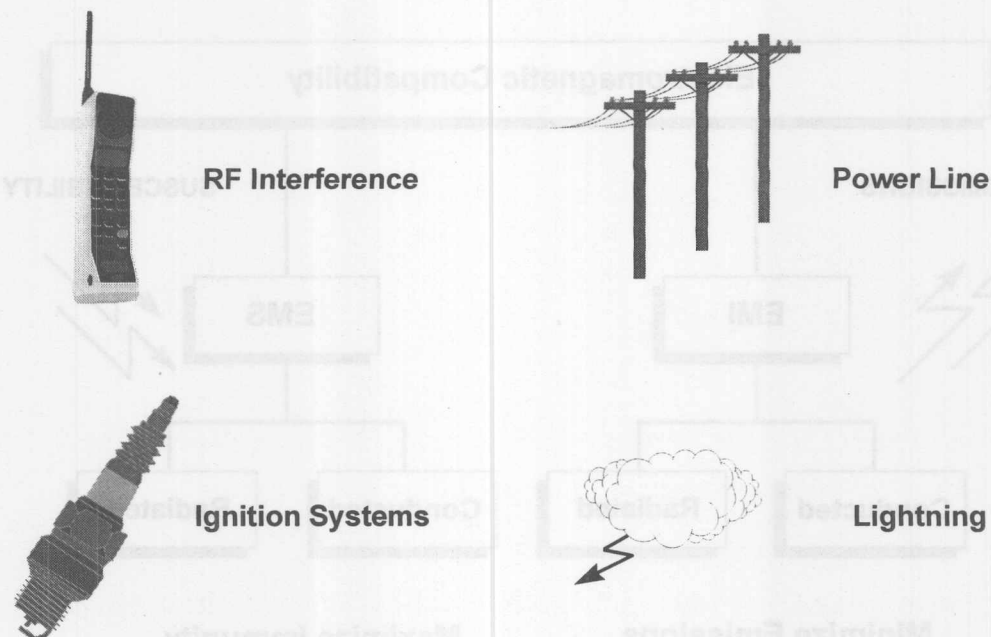
EMC on Interface Products - Why is it so Important?



- **I-O Transceiver Is Directly in the Firing Line for Transients - RS-232 Port Is Particularly Vulnerable**
- **I-O Port Is an Open Gateway in the Enclosure**
- **Harmonised Standards Are Now Mandatory Requirements in European Community**

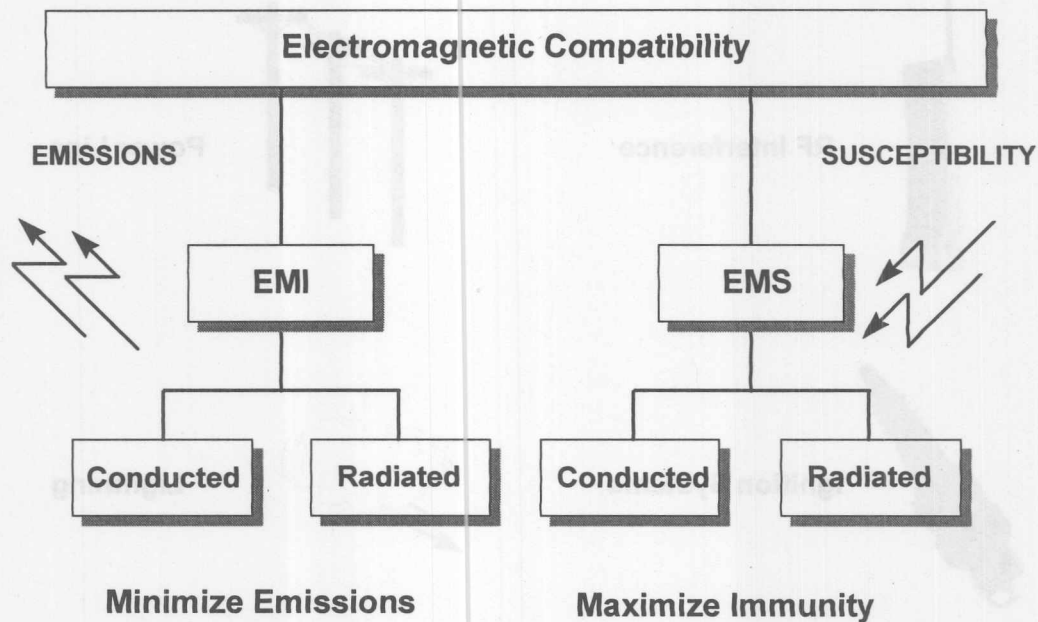


Sources of EMI



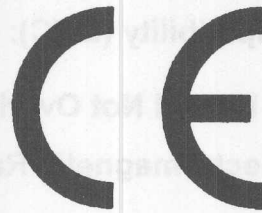


EM Compatibility





European Requirements - the CE Mark



- **EMC Compatibility**
- **EM Emissions**
- **EM Immunity**
 - **ESD**
 - **EFT**



ElectroMagnetic Compatibility - Definitions

- **Electromagnetic Compatibility (EMC):**
 - **Ability to Operate in, and Not Overly Contribute to, an Environment of Electromagnetic Radiation**
- **Electromagnetic Interference (EMI) :**
 - **Electromagnetic Energy Emanating From One Device Causing Degraded Performance in Another**
- **Electromagnetic Immunity (Susceptibility, EMS) :**
 - **Tolerance in the Presence of Electromagnetic Energy**



Who Must Comply with the EMC Directive?

- **Manufacturers of Electronic Equipment for:**
 - **Information Technology equipment (ITE)**
 - **Industrial, Scientific, Medical**
 - **Broadcast Receivers**
 - **Household, Appliances, Tools**
 - **Fluorescent Lamps and Luminaries**
 - **Signaling on Power Lines**
- **For Use In:**
 - **Residential/Commercial Environments**
 - **Commercial Environments**
 - **Industrial Environments**

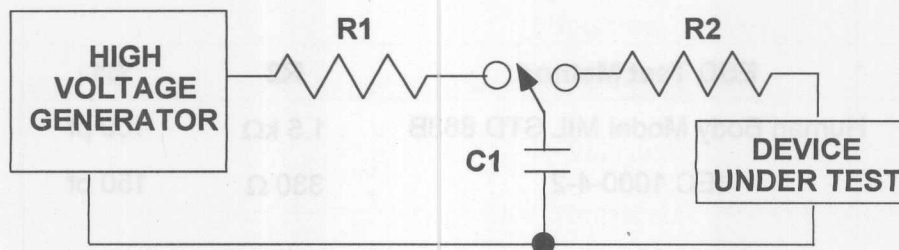


IEC 1000-4-x Basic Immunity Standards

- **Current Reference Section**
- **IEC1000-4 Electromagnetic Compatibility EMC**
- **IEC1000-4-1 Overview of Immunity Tests**
- **IEC1000-4-2 Electrostatic Discharge Immunity (ESD)**
- **IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity**
- **IEC1000-4-4 Electrical Fast Transients (EFT)**
- **IEC1000-4-5 Lightning Surges**
- **IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz**



ESD Test Method IEC1000-4-2

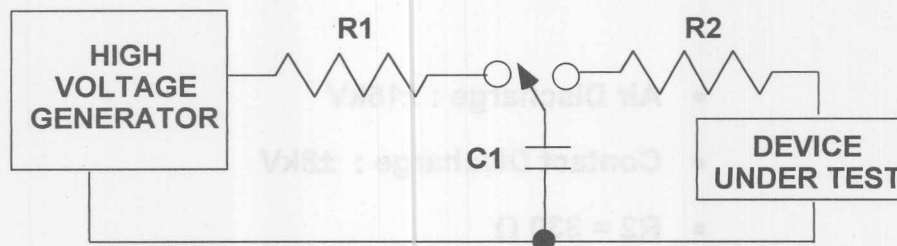


- Air Discharge : $\pm 15\text{kV}$
- Contact Discharge : $\pm 8\text{kV}$
- $R2 = 330\ \Omega$
- $C1 = 150\ \text{pF}$



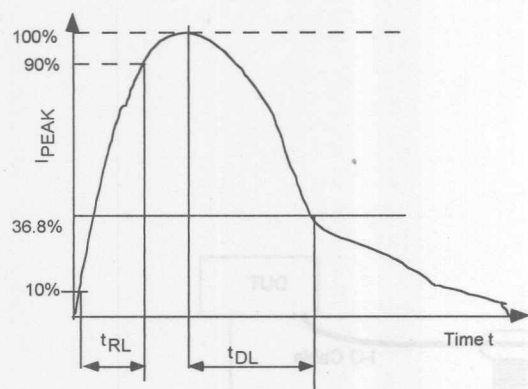
IEC1000-4-2 vs. HBM Testing

ESD Test Method	R2	C1
Human Body Model MIL STD 883B	1.5 k Ω	100 pf
IEC 1000-4-2	330 Ω	150 pf

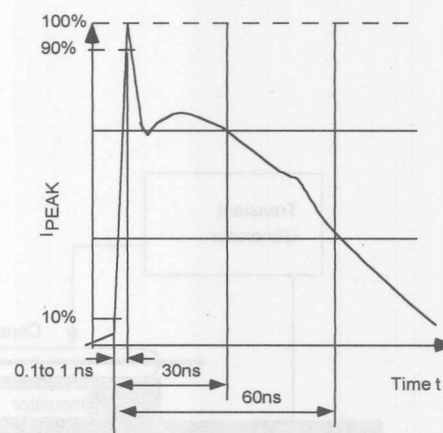




ESD Discharge Waveforms



HBM

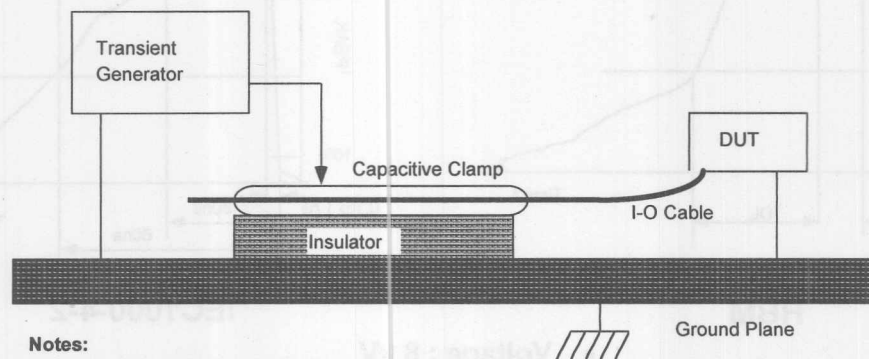


IEC1000-4-2

- Voltage : 8 kV
- Peak Current :
 - IEC : 25 A
 - HBM : 5 A



EFT Testing

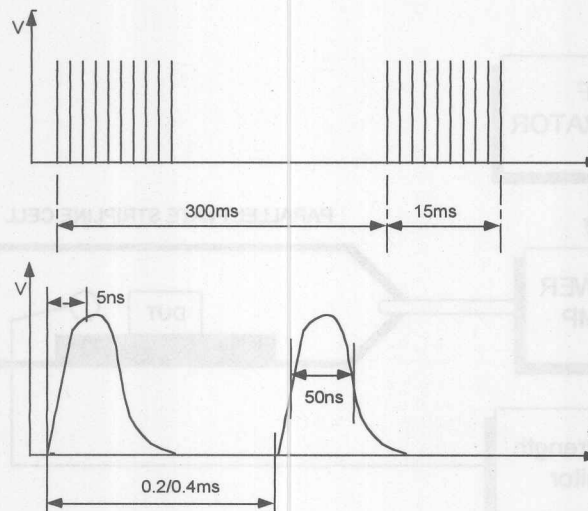


Notes:

Transients up to 2kV Positive and Negative
Device is Powered-Up and Transmitting Data



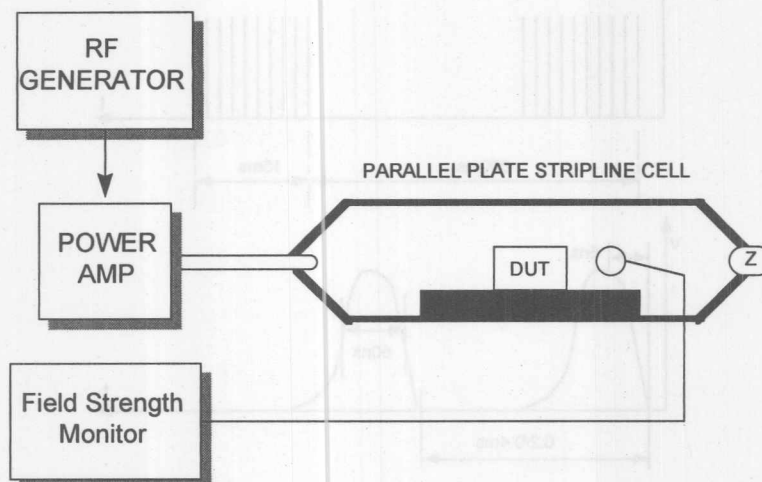
IEC1000-4-4 EFT



- IEC 1000-4-4 (Previously 801-4)
- EFT Fast Transient Burst Test
- Applied to 1 meter Cable Connected to I-O Lines



1000-4-3 Electric Field Immunity



DUT is paced within an electric field

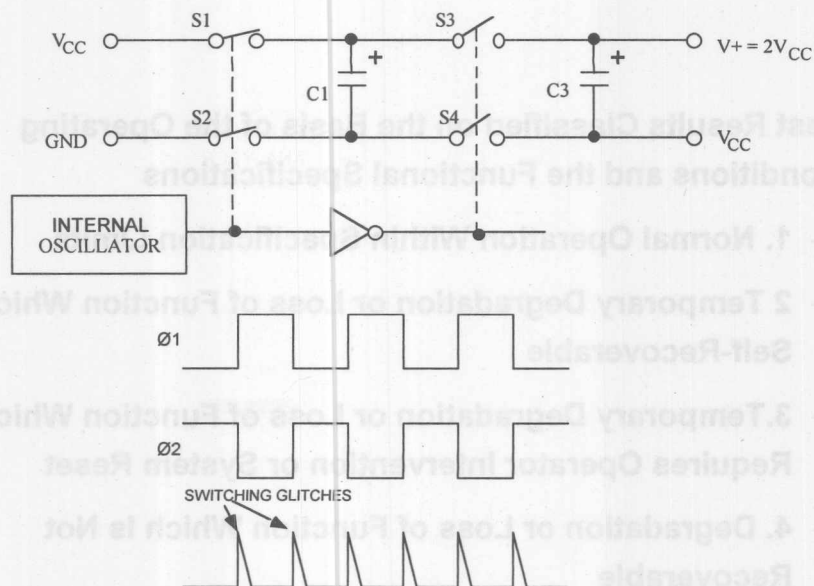


Classification of Results

- **Test Results Classified on the Basis of the Operating Conditions and the Functional Specifications**
 - **1. Normal Operation Within Specification Limits**
 - **2 Temporary Degradation or Loss of Function Which Is Self-Recoverable**
 - **3. Temporary Degradation or Loss of Function Which Requires Operator Intervention or System Reset**
 - **4. Degradation or Loss of Function Which Is Not Recoverable**



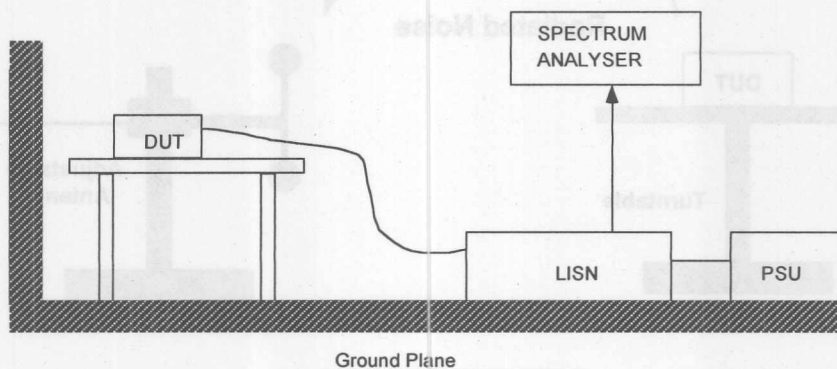
Source of Conducted Emissions



7-18



Conducted Emissions - Testing

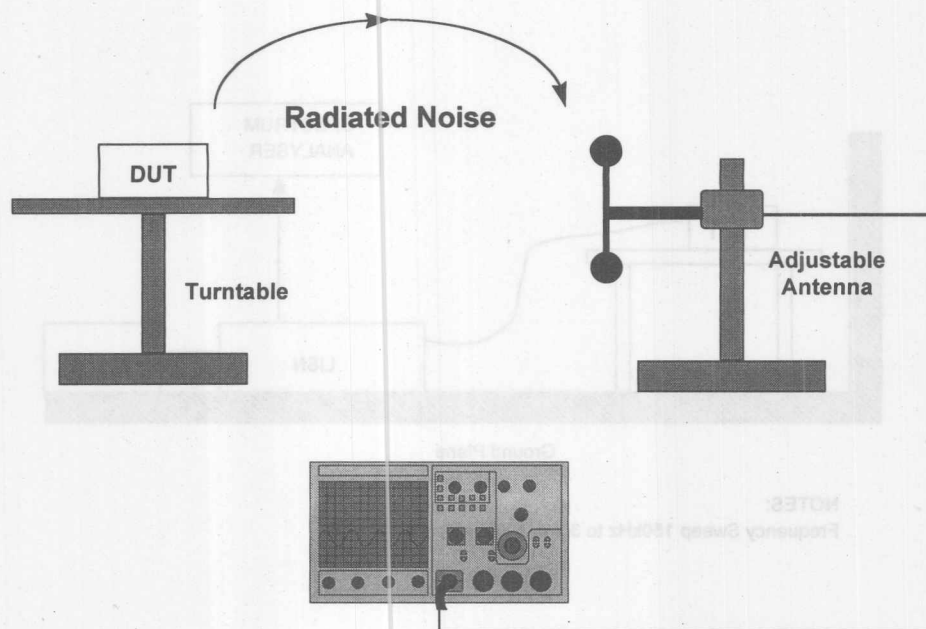


NOTES:
Frequency Sweep 150kHz to 30MHz BW = 9kHz

7 - 19



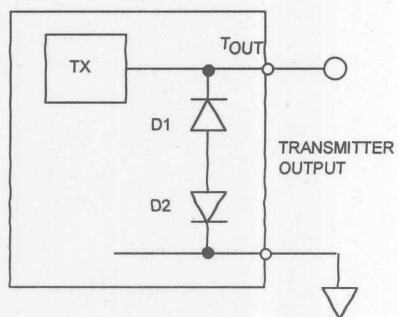
Radiated Emissions Test Setup



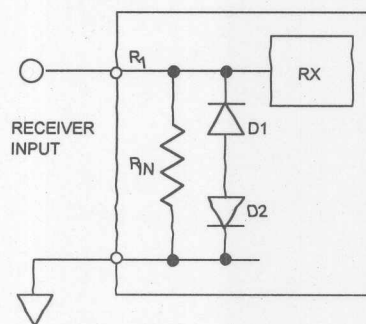
7 - 20



ESD/EFT Protection



**Transmitter Output
Protection Structure**



**Receiver Input
Protection Structure**

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RS-232E Line Drivers/Receivers



ADM1385, ADM3202 and ADM3222 3V, Low Power RS-232 Transceivers

The ADM1385, ADM3202 and ADM3222 are improved performance upgrades to the LTC1385 and the MAX3222 and MAX3232.

- 2 Drivers and 2 Receivers
- 230 kbits Data Rate Guaranteed!
- Conform to EIA-232E and CCITT V.28
- +3.0 V to +3.6 V Operation
- 2 mA Quiescent Current
- 0.1 uA Shutdown Current (ADM1385, ADM3222)
- 0.1 uF External Charge Pump Capacitors
- ADM1385 : 20 pin SSOP
- ADM3202 : 16 pin DIP, SOIC and TSSOP
- ADM3222 :
 - 18 Pin DIP, SOIC
 - 20 Pin SSOP, TSSOP

7-24

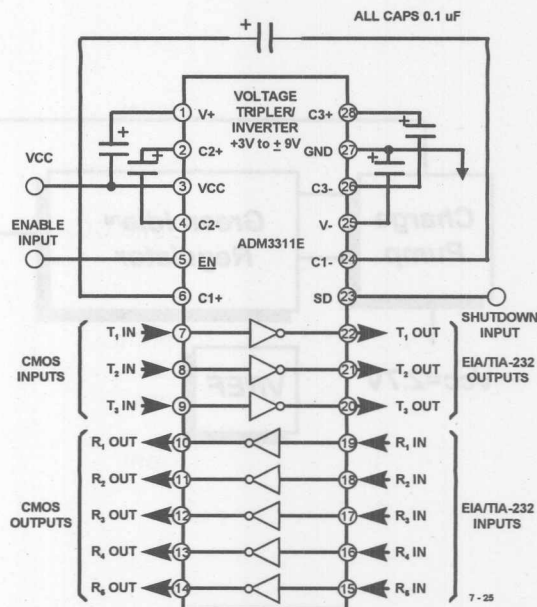


ADM3311E

Serial Port RS-232 Driver/Receiver

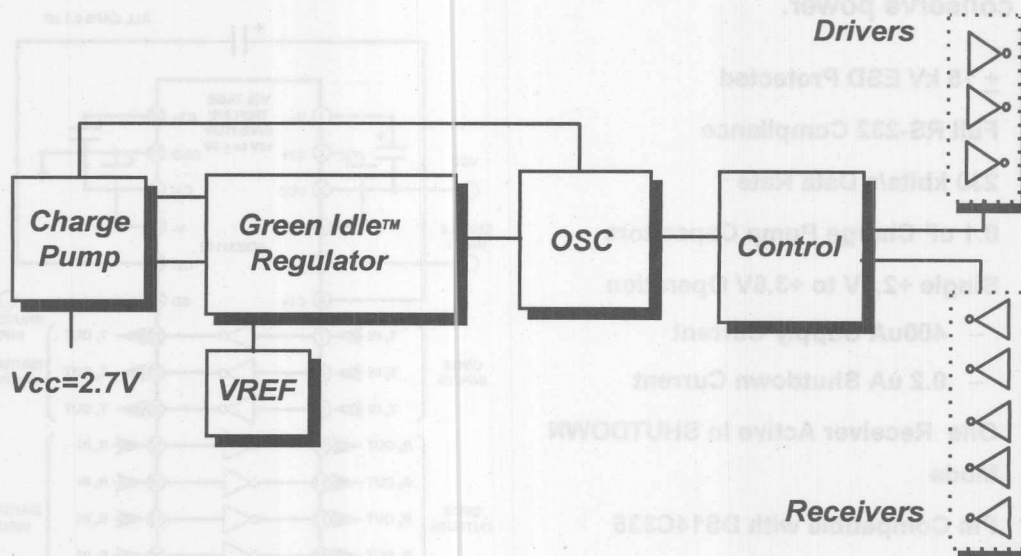
The ADM3311E features a patented Green-Idle™ power saving mode whereby the internal oscillator idles at a minimum frequency to conserve power.

- ± 15 kV ESD Protected
- Full RS-232 Compliance
- 230 kbits/s Data Rate
- 0.1 μ F Charge Pump Capacitors
- Single +2.7V to +3.6V Operation
 - 400 μ A Supply Current
 - 0.2 μ A Shutdown Current
- One Receiver Active in SHUTDOWN Mode
- Pin Compatible with DS14C335
- 28 Pin TSSOP Package





ADM3311 Architecture with Green Idle™



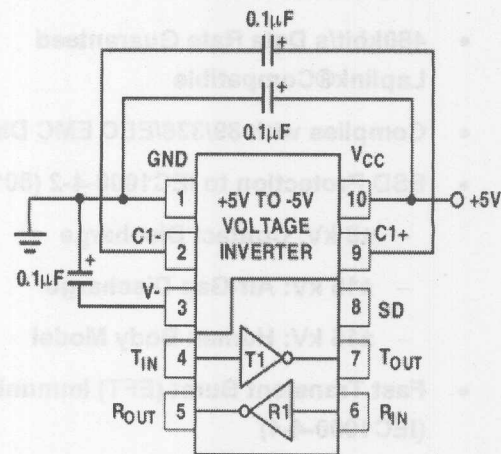
7-26



ADM101E

CraftPort™ RS-232E Driver/Receiver

- 1 Driver/ 1 Receiver
- Voltage Inverter Only
- Single 5V Supply
- RS232 Compatible
- Shutdown Mode
- 10 Lead μ SOIC Package



7-27

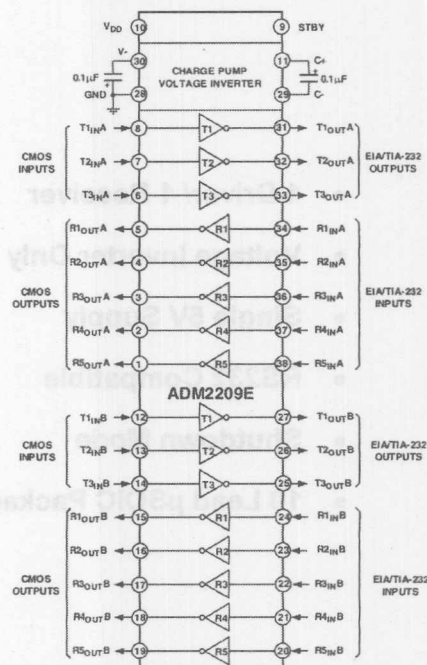


Preliminary
Information

ADM2209E*

RS-232E Driver/Receiver for Desktops

- Two Complete Serial Ports, 6 Drivers and 10 Receivers
- 460kbit/s Data Rate Guaranteed
Laplink®Compatible
- Complies with 89/336/EEC EMC Directive
- ESD Protection to IEC1000-4-2 (801.2)
 - ±8 kV: Contact Discharge
 - ±15 kV: Air-Gap Discharge
 - ±15 kV: Human Body Model
- Fast Transient Burst (EFT) Immunity (IEC1000-4-4)
- Low EMI Emissions (EN55022)
Eliminates Costly TransZorbs*

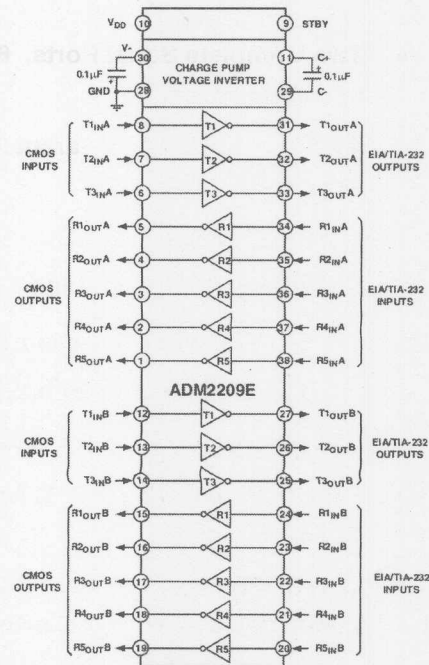


7 - 28

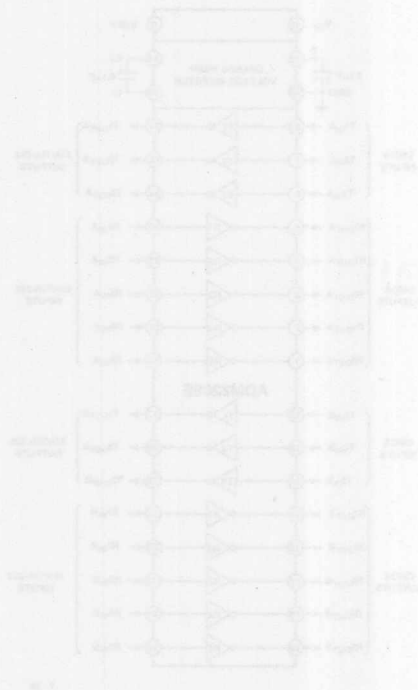


ADM2209E

- Operates with 3V or 5V Logic
- Low Power CMOS: 2mA Operation
- Low Standby Current: 100 μ A
- 0.1 μ F Charge Pump Capacitors
- Single +12V Power Supply
- +3V to +5V Standby Supply
- One Receiver on each Port Active in Standby



7 - 29



- Operates with 3V or 5V Logic
- Low Power CMOS: 2mA Operation
- Low Standby Current: 100µA
- 0.1µF Charge Pump Capacitors
- Single +12V Power Supply
- +3V to +5V Standby Supply
- One Receiver on each Port Active in Standby

7-30



RS-485 Transceivers

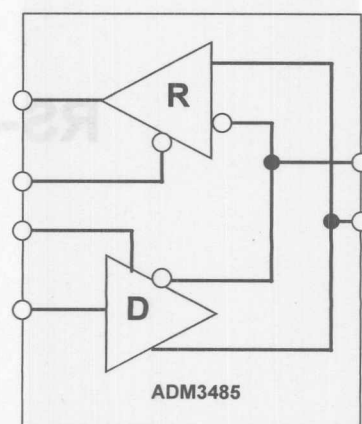




ADM3485E **3.3V, 20 Mbps EIA RS-485 Transceiver**

The ADM3485E is an improved upgrade to the MAX3485

- EIA RS-422 and RS-485 Compliant over the full CM Range
- 20 Mbps Data Rate
- ESD Protection : 8 kV (IEC1000-4-2)
- EFT Protection : 2 kV (IEC1000-4-4)
- 8 ns Skew

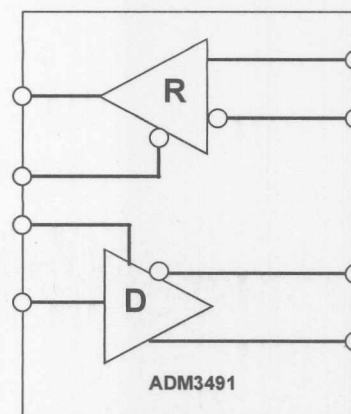


7 - 32



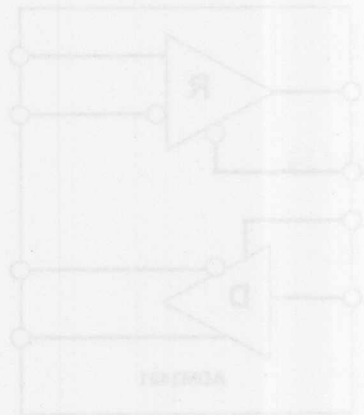
ADM3485E (con't)

- Interoperable with 5V Logic
- 19 k ohms Input Impedance Allows Up to 50 Tranceivers on Bus
- Short Circuit Protection
- Thermal Shutdown
- < 1 mA Supply Current
- 2 nA Shutdown Current
- 8 Pin DIP, SOIC Packages



7-33

ADM3485E (cont.)

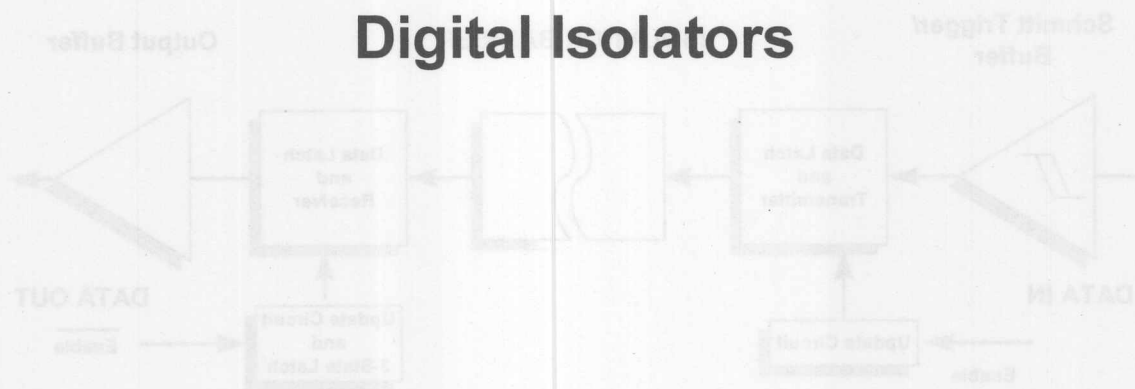


- Interoperable with 5V Logic
- 19 k ohms Input Impedance Allows Up to 80 Transceivers on Bus
- Short Circuit Protection
- Thermal Shutdown
- < 1 mA Supply Current
- 2 mA Shutdown Current
- 8 Pin DIP, SOIC Packages

7-34



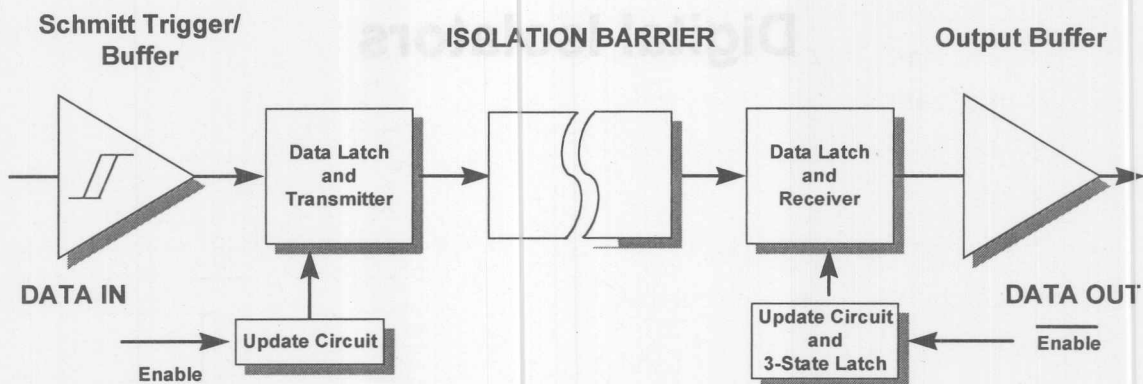
Digital Isolators





AD260, AD261 High Speed, High Voltage Digital Logic Isolators

The AD260 and AD261 are 5 channel, high speed logic isolators capable of providing > 4 kV of isolation between a microcontroller's high speed digital I/O lines and its related field I/O components.

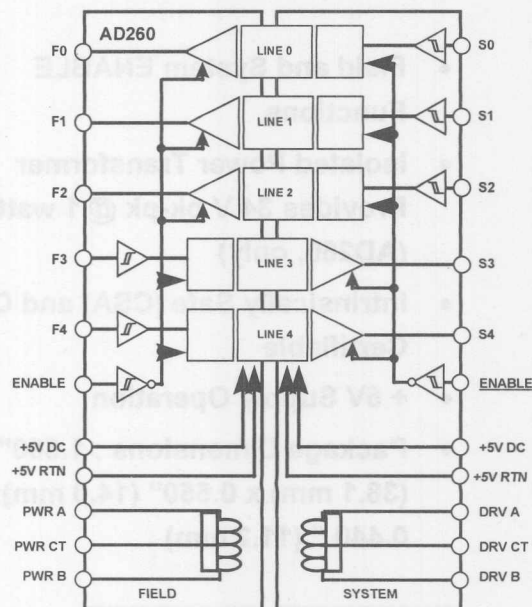


7-36



AD260 and AD261 Key Specs and Features

- 3.5 kV Isolation Voltage Range
- Up to 10 kV/us CMV Transient Immunity
- 5 HCMOS-Compatible Isolated Logic Lines : Available in 6 I/O Configurations
- 20 MHz Minimum Logic Signal Bandwidth
- 11 ns Propagation Delay
- Rise and Fall Time Symmetry : ± 2 ns

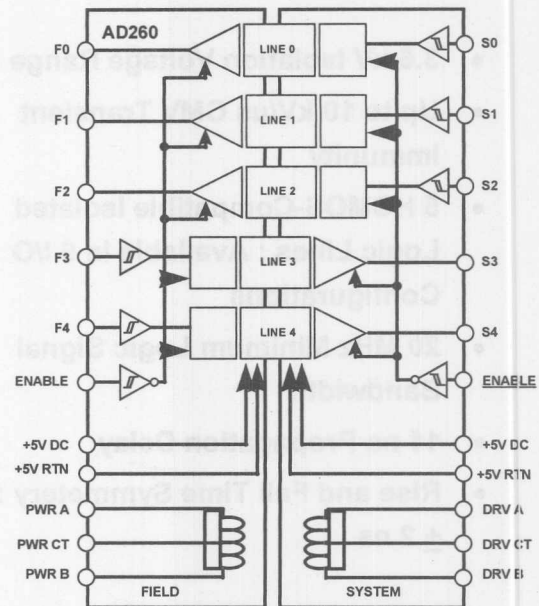


7 - 37



AD260 and AD261 Key Specs and Features (con't)

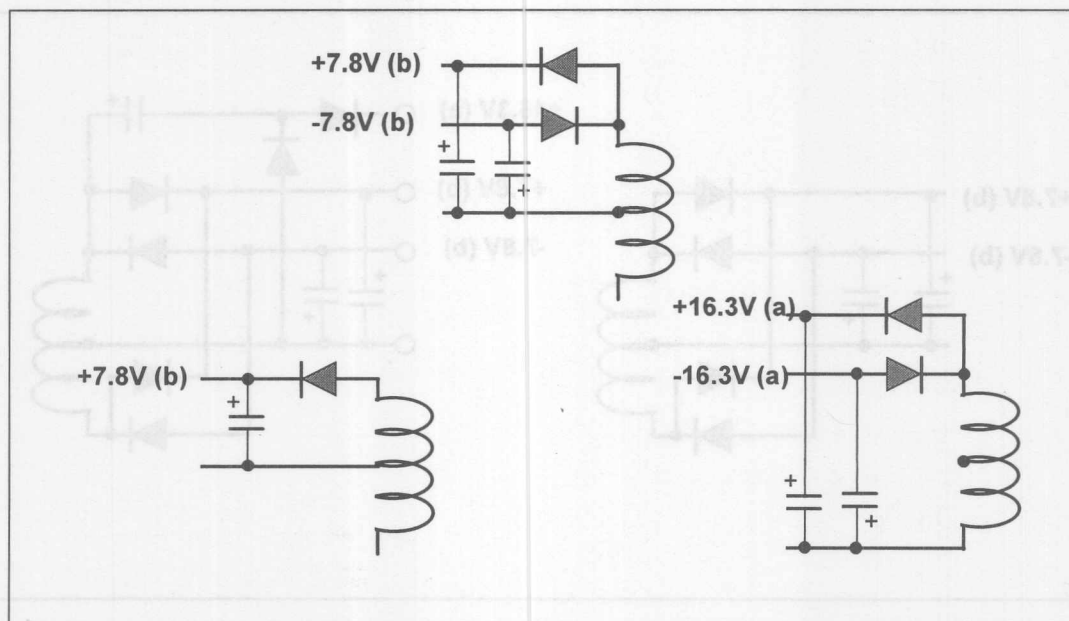
- Field and System ENABLE Functions
- Isolated Power Transformer Provides 34 V pk-pk @ 1 watt (AD260, only)
- Intrinsically Safe (CSA) and CE Certifiable
- + 5V Supply Operation
- Package Dimensions : 1.500" (38.1 mm) x 0.550" (14.0 mm) x 0.440" (11.2 mm)



7 - 38



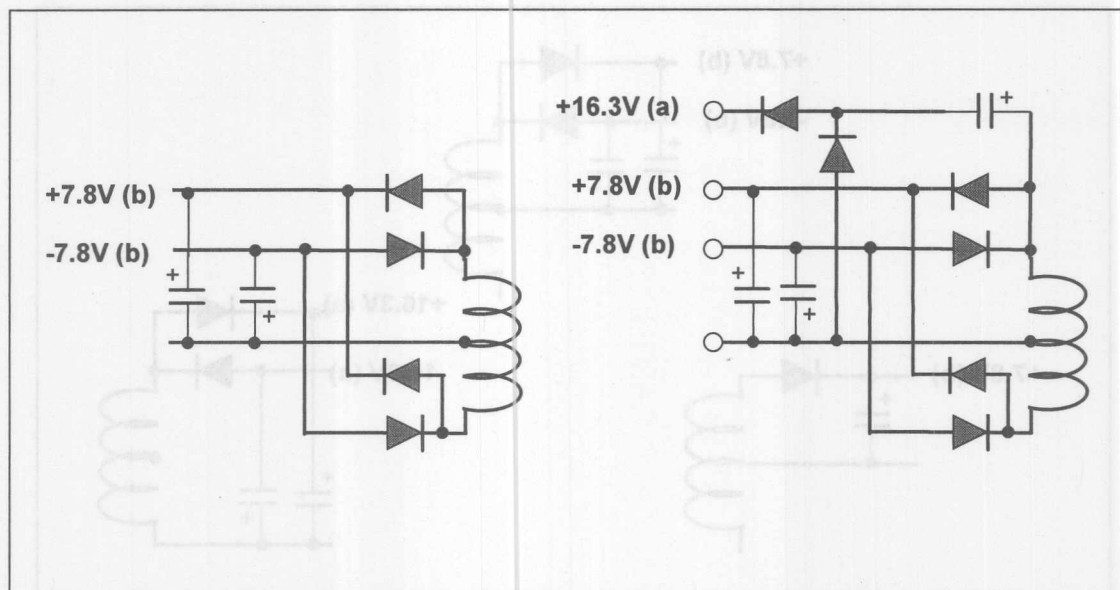
AD260 Isolated Transformer - Typical Drive and Regulation (con't)



7 - 39



AD260 Isolated Transformer - Typical Drive and Regulation (con't)



7-40



AD260, AD261 - Ordering Guide

Model Number	Model Number	Inputs	Outputs
AD260BND-0	AD261CND-0	0	5
AD260BND-1	AD261CND-1	1	4
AD260BND-2	AD261CND-2	2	3
AD260BND-3	AD261CND-3	3	2
AD260BND-4	AD261CND-4	4	1
AD260BND-5	AD261CND-5	5	0



Model Number	Model Number	Inputs	Outputs
AD2808ND-0	AD281CND-0	0	8
AD2808ND-1	AD281CND-1	1	4
AD2808ND-2	AD281CND-2	2	3
AD2808ND-3	AD281CND-3	3	2
AD2808ND-4	AD281CND-4	4	1
AD2808ND-5	AD281CND-5	5	0



SECTION 8 POWER MANAGEMENT PRODUCTS

Linear Voltage Regulators

Low Drop Out (LDO) Regulators

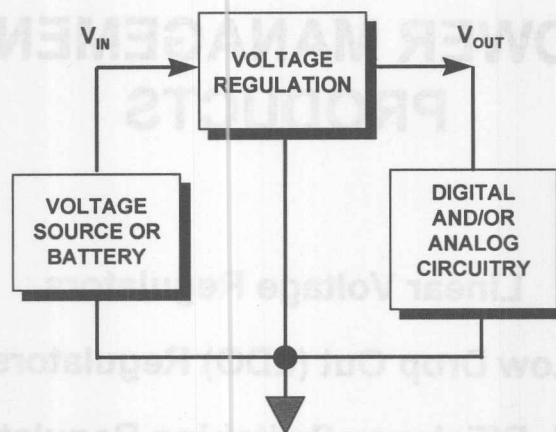
High Efficiency Switching Regulators

Charge Pump Converters

Battery Charger Controllers



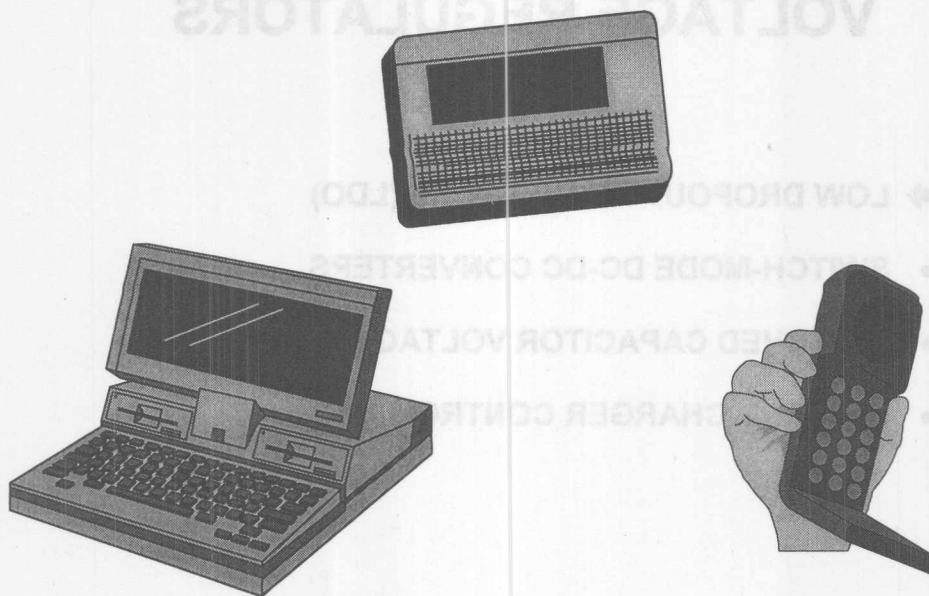
What is Power Management?



- Maintain Constant V_{OUT} Under Varying Load Conditions or Varying V_{IN}
- Reduce the Number of Independent Power Supplies
- V_{OUT} Can Be Greater Than V_{IN} (Step Up : e.g., 5V \rightarrow 12V)
- V_{OUT} Can Be Less Than V_{IN} (Step Down : e.g., 12V \rightarrow 5V)
- “DC - DC Converters”



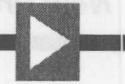
The World is Going Mobile/Portable = Battery Powered...





VOLTAGE REGULATORS

- ➔ **LOW DROPOUT REGULATORS (LDO)**
- **SWITCH-MODE DC-DC CONVERTERS**
- **SWITCHED CAPACITOR VOLTAGE CONVERTER**
- **BATTERY CHARGER CONTROLLERS**



Why Linear Regulators?

- **Simple to Use**
- **Improved Transient Response**
- **Fewer Components**
- **No EMI, RFI**
- **but.....**
- **Less Efficient Than a Switcher**
- **Generates More Heat**

8-5



Analog Devices **anyCAP™*** **LDO (Low Drop Out)** **Regulators**

***anyCAP is a trademark of Analog Devices Inc.**



Analog Devices anyCAP™ LDO - Regulators

Typical LDO's lack sufficient phase margin, and to remain stable require output capacitors with a minimum ESR. To obtain the required ESR, designers are forced to use more costly and larger caps. Additionally the ESR of a Capacitor varies with temperature requiring further circuit design analysis. Analog Devices anyCAP™ LDO's use internal pole splitting to eliminate the need for minimum ESR. Analog Devices anyCAP™ LDO's are stable with any type of capacitor including MLCC's, with values as low as 0.47uF.



Typical LDOs vs ADI's anyCAP™ LDO

anyCAP™ LDOs

- No Min. ESR Requirement
- No Stability Problems
- Less Design Effort
- Smaller Size Capacitor
- Smaller Value Capacitor
- Less Board Space
- Lower Cost Capacitor

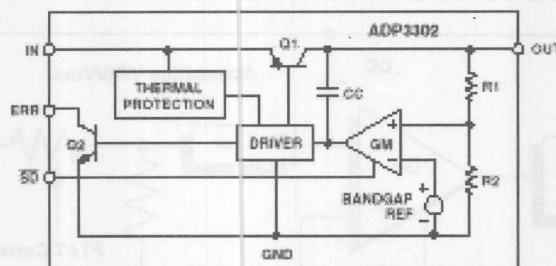
Conventional LDOs

- Min. ESR Required
- Can Become Unstable
- More Design Effort
- Larger Value Capacitor
- Larger Size Capacitor
- More Board Space
- Higher Cost Capacitor

8-8



ADP3302 anyCAP™ Dual Output - Low Dropout Linear Regulator



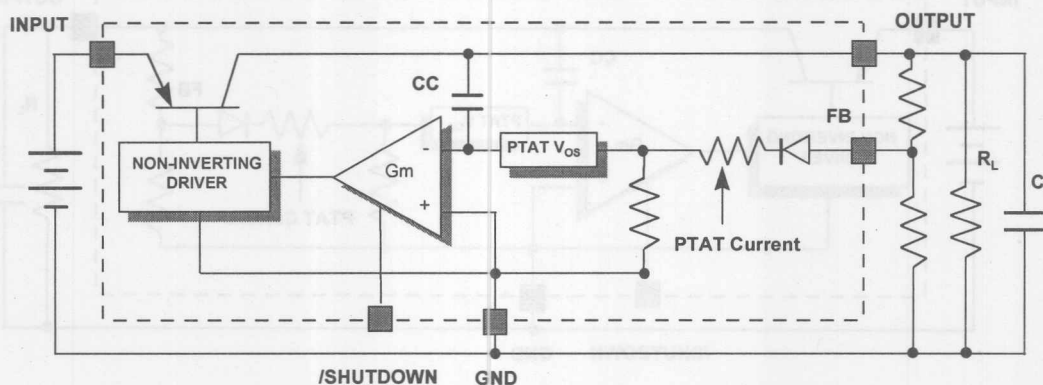
(1 OF 2 CHANNELS SHOWN)

- Dual Output LDO
- 120 mv Typical Dropout Voltage @ $I_L = 100 \text{ mA}$.
- 3.0 V to 12 V Input Voltage Range
- 3.0, 3.2, 3.3 and 5.0 Volt Output Voltages @ 100mA Each

8-10



ADP3303A anyCAP™ Adjustable 200mA LDO Regulator



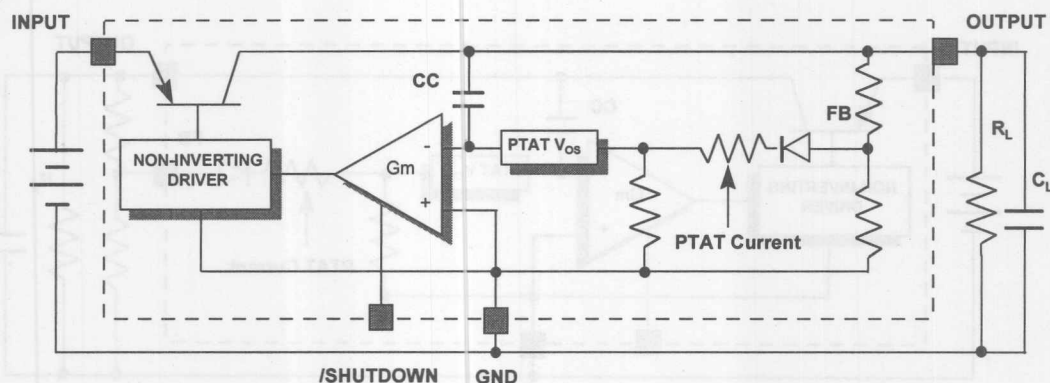
- Resistor Programmable Output Voltage 2.2V to 10V
- Wide Input Voltage Range 3.2V to 12V
- 150 mV. Typical Dropout Voltage @ $I_L = 200 \text{ mA}$.
- TSSOP - 14 Package

8-11



EDN Magazine
Innovation of the year Finalist

ADP3330 anyCAP™ SOT23-6 200mA LDO Regulator

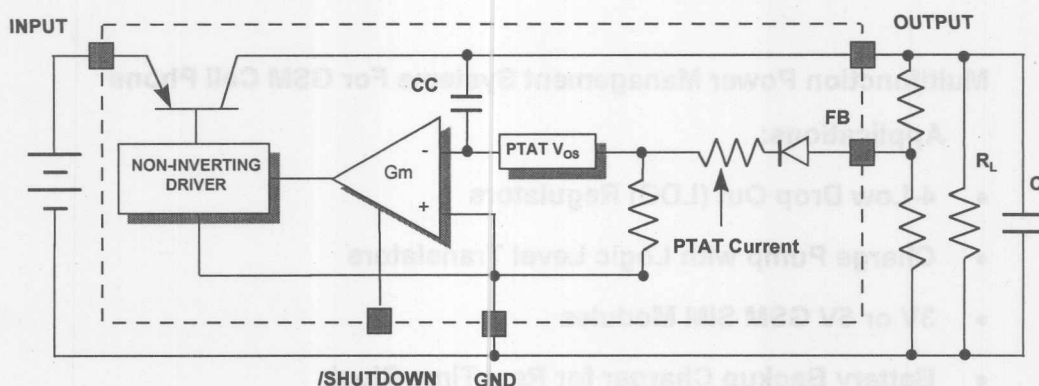


- High Accuracy: $\pm 0.7\%$ Over Line and Load
- Fixed Output Voltages: 2.5V, 2.75V, 2.85V, 3.0V, 3.3V and 3.6V
- Wide Input Voltage Range 2.9V to 12V
- Ultra Low Dropout 150 mV. Typical @ $I_L = 200$ mA.
- SOT23 - 6 - Ultra Small Package

8-12



ADP3331 anyCAP™ Adjustable 200mA LDO Regulator



- Adjustable Output Voltages 1.5V - 10.0V
- Wide Input Voltage Range 3.2V to 12V
- 150 mV. Typical Dropout Voltage @ $I_L = 200$ mA.
- SOT23 - 6 Package

8 - 13



**Preliminary
Information**

ADP3401 / ADP3402 GSM Power Management System

Multifunction Power Management Systems For GSM Cell Phone

Applications:

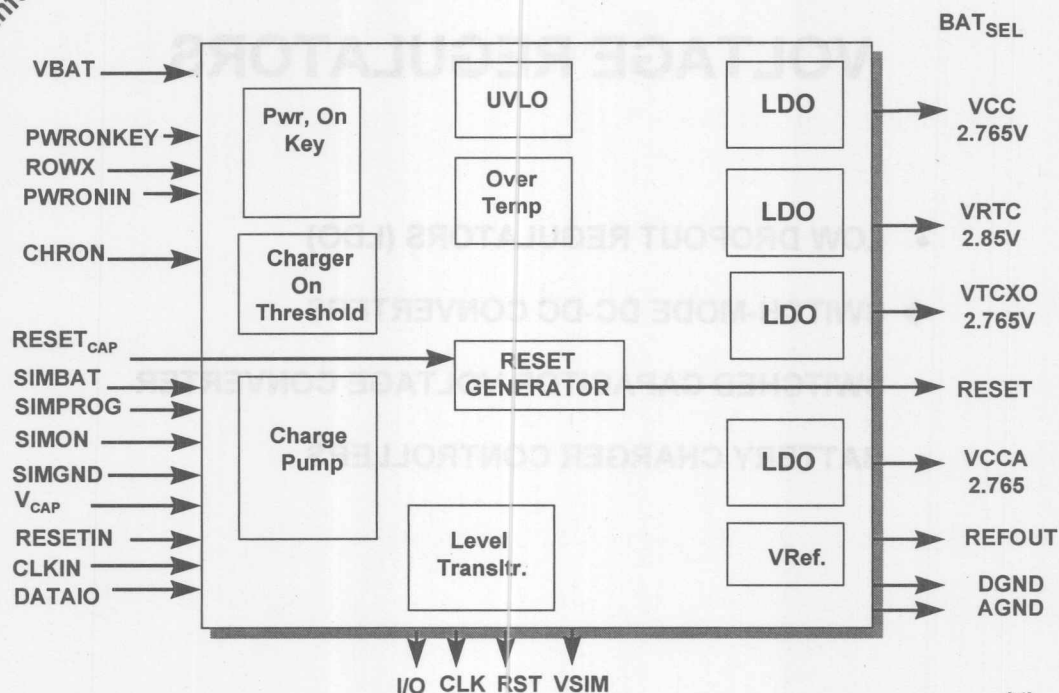
- **4-Low Drop Out (LDO) Regulators**
- **Charge Pump with Logic Level Translators**
- **3V or 5V GSM SIM Modules**
- **Battery Backup Charger for Real Time Clock**
- **Power Up Sequencing**
- **Thermally Enhanced 28 Pin TSSOP Package**
- **Optimized For Use With Analog Devices AD20msp425 Chipset**

8-14



Preliminary
Information

ADP3401/ ADP3402 GSM Cell Phone Power Management System



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VOLTAGE REGULATORS

- LOW DROPOUT REGULATORS (LDO)
- ➔ SWITCH-MODE DC-DC CONVERTERS
- SWITCHED CAPACITOR VOLTAGE CONVERTER
- BATTERY CHARGER CONTROLLERS



Specifying Switch Mode DC-DC Converters (Switching Regulators)

BY FUNCTION:

- Step Down = "Buck"
- Step Up = "Boost"
- Step Up/Down = Buck/Boost
- Invert = Negative Buck/Boost

BY CONTROL METHOD:

- Voltage Mode
- Current Mode
- Pulse Width Modulation

BY MAGNETICS:

- Transformer:
 - Flyback
 - Forward
 - Push - Pull
- Inductor:
 - Buck
 - Boost
 - Buck/Boost

8 - 17

How to Choose a Switching Regulator

- **Output Current:**
 - Can It Supply Enough Current for the Circuit
(From 1.0 mA to a Few Amps)
- **Switching Speed:**
 - Directly Determines the Size of the Inductor,
the Higher the Speed, the Smaller the
Inductor (75 kHz to 400 kHz)
- **Required Inductor:**
 - The Smaller the Better Due to Size and Cost.
(10Mh to 120Mh Typical Values)

8-18



How to Choose a Switching Regulator (con't)

- **Efficiency:**
 - The Higher the Better (> 90% Is Typical)
- **Output Noise :**
 - Switchers Generate Output Ripple and Radiated EMI. The Lower the Better.
- **Features:**
 - Shutdown - Saves Power and Lower Noise



**Preliminary
Information**

ADP3020, ADP3021 Power Management for Laptop / Notebook Computer

- **Complete Power Management System on a Chip for Laptop and Notebook Computers**
- **Wide Input Voltage Range 5.5V to 25V with >95% Efficiency**
- **Dual Voltage Mode PWM Synchronous N-Channel Buck Converters with LDO Converter and Overvoltage Protection**
- **Optimized for the Next Generation Pentium III* and the AMD** K6-2 Processors**
- **Low Quiescent Current 400uA. Operating 100uA. Standby**
- **Power Fail Monitoring ADP3020**
- **User Programmable Current Limit**
- **38 Lead TSSOP Package**

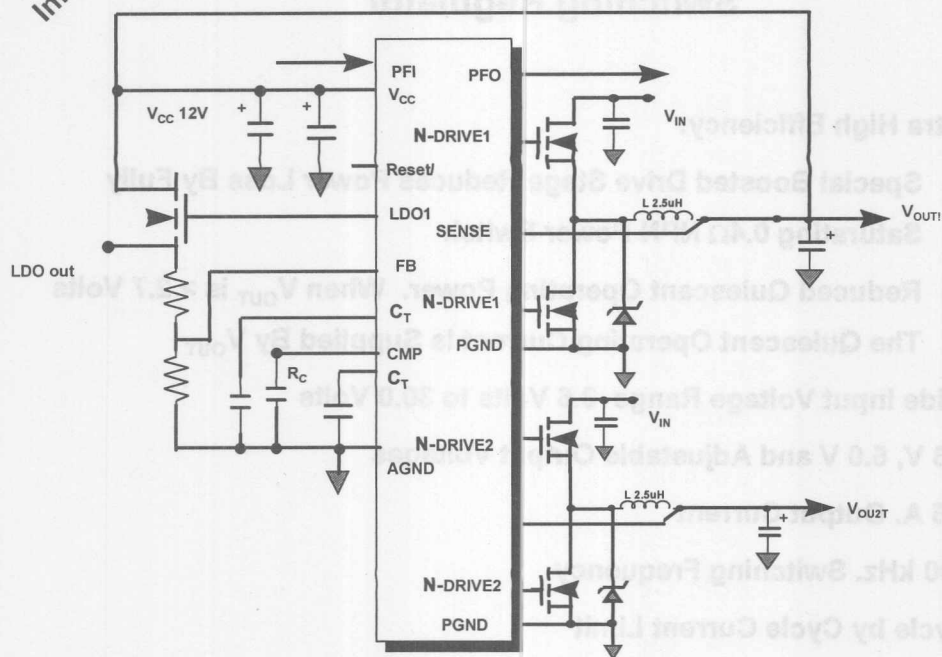
8 - 20



Preliminary
Information

ADP3020 / ADP3021

Laptop / Notebook Computer Application



8 - 21



Preliminary
Information

ADP3050 High Efficiency 1.5 A. Step - Down Switching Regulator

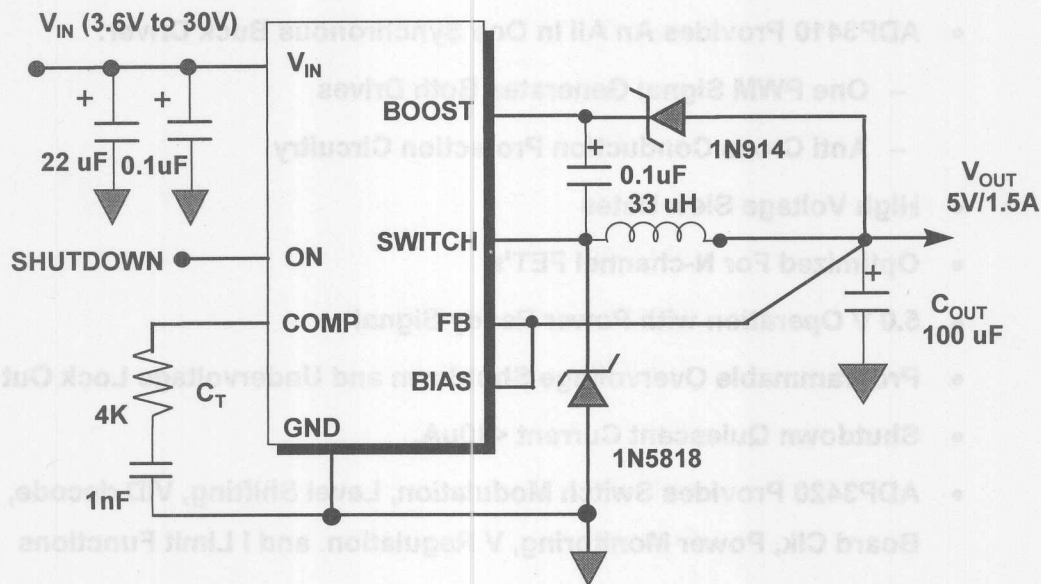
- Ultra High Efficiency:
 - Special Boosted Drive Stage Reduces Power Loss By Fully Saturating 0.4Ω NPN Power Switch
 - Reduced Quiescent Operating Power. When V_{OUT} is > 2.7 Volts The Quiescent Operating Current Is Supplied By V_{OUT}
- Wide Input Voltage Range 3.6 Volts to 30.0 Volts
- 3.3 V, 5.0 V and Adjustable Output Voltages
- 1.5 A. Output Current
- 300 kHz. Switching Frequency
- Cycle by Cycle Current Limit

8 - 22



Preliminary
Information

ADP3050 High Efficiency 1.5 A. Step - Down Switching Regulator



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Preliminary
Information

ADP3410 / ADP3420 High Speed Synchronous MOSFET Driver

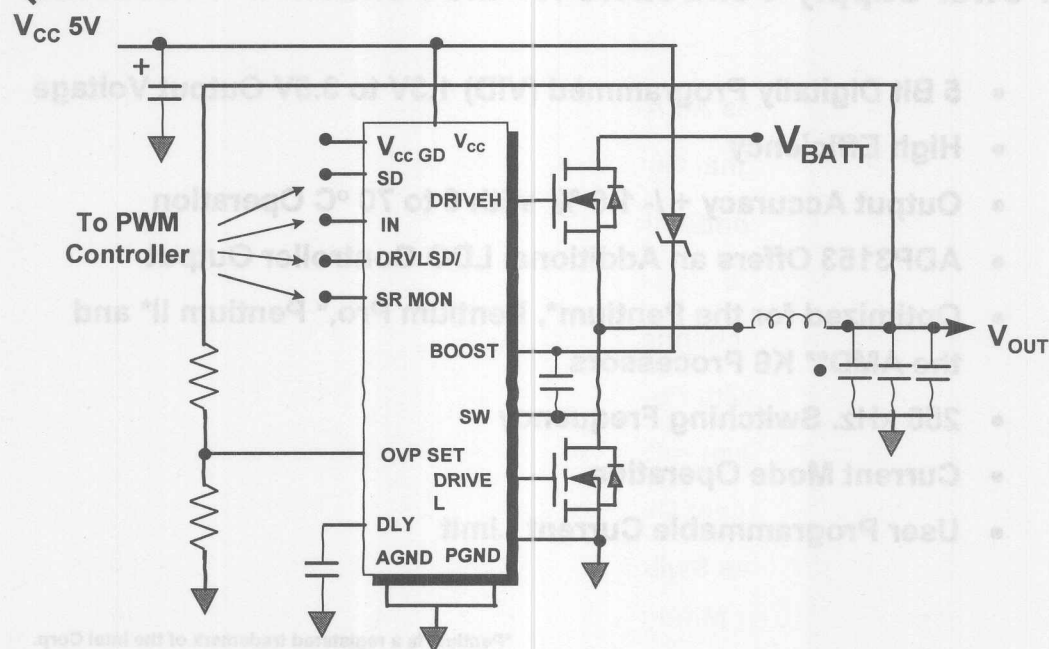
- ADP3410 Provides An All In One Synchronous Buck Driver:
 - One PWM Signal Generates Both Drives
 - Anti Cross Conduction Protection Circuitry
- High Voltage Slew Rates
- Optimized For N-channel FET's
- 5.0 V Operation with Power Ready Signal
- Programmable Overvoltage Shutdown and Undervoltage Lock Out
- Shutdown Quiescent Current $<10\mu\text{A}$.
- ADP3420 Provides Switch Modulation, Level Shifting, VID decode, Board Clk, Power Monitoring, V Regulation. and I Limit Functions

8 - 24



Preliminary
Information

ADP3410 High Speed Synchronous MOSFET Driver



8 - 25

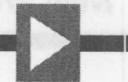


ADP3152, ADP3153
5 Bit VID Code Programmable
Power Supply Controllers for the Pentium II* Processor

- 5 Bit Digitally Programmed (VID) 1.3V to 3.5V Output Voltage
- High Efficiency
- Output Accuracy + /- 1.0 % with 0 to 70 °C Operation
- ADP3153 Offers an Additional LDO Controller Output
- Optimized for the Pentium*, Pentium Pro,* Pentium II* and the AMD** K6 Processors
- 250 kHz. Switching Frequency
- Current Mode Operation
- User Programmable Current Limit

*Pentium is a registered trademark of the Intel Corp.
** Advanced Micro Devices Inc

8 - 26



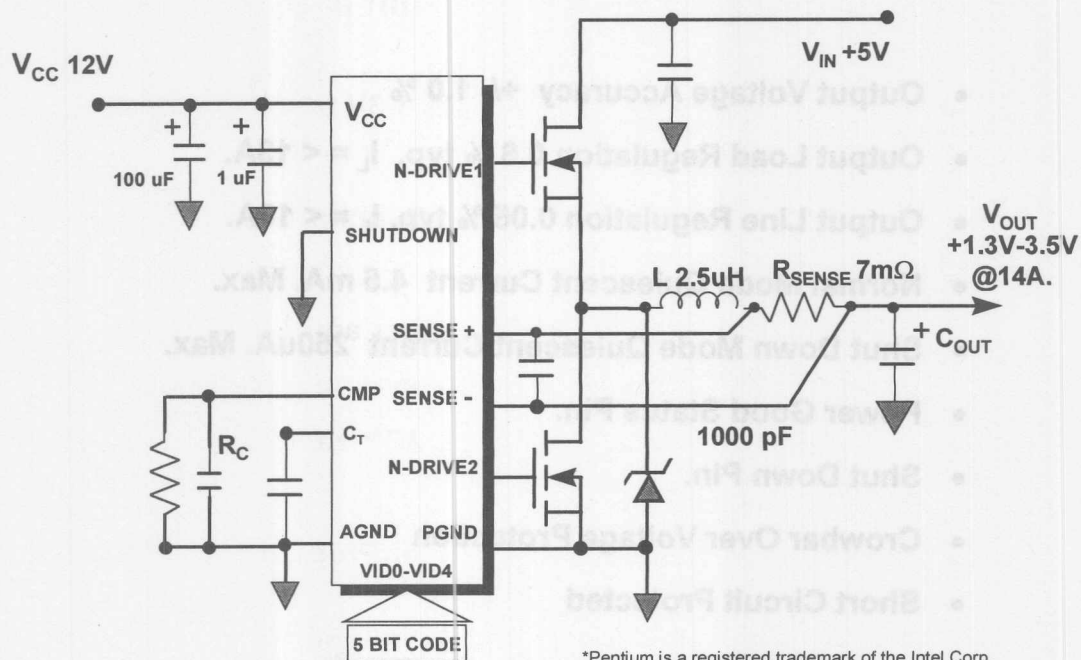
ADP3152, ADP3153 Additional Specifications

- Output Voltage Accuracy $\pm 1.0\%$
- Output Load Regulation 0.6% typ. $I_L = < 13A$.
- Output Line Regulation 0.05% typ. $I_L = < 10A$.
- Normal Mode Quiescent Current 4.5 mA . Max.
- Shut Down Mode Quiescent Current $250\mu A$. Max.
- Power Good Status Pin.
- Shut Down Pin.
- Crowbar Over Voltage Protection
- Short Circuit Protected

8-27



ADP3152, ADP3153 5 Bit VID Programmable Output Converter for Pentium II* Processors



*Pentium is a registered trademark of the Intel Corp.

8 - 28



ADP3154, ADP3155
5 Bit VID Code Programmable Dual and Triple
Controllers for the Pentium II* Processor

- 5 Bit Digitally Programmed (VID) 1.3V to 3.5V Output
- VRM 8.2, 8.3, and 8.4 Compatible
- High Efficiency Dual N-Channel Synchronous Drivers
- Output Accuracy + /- 1.0 % with 0 to 70 °C Operation
- ADP3154 Dual Controller: Switcher and LDO Output
- ADP3155 Triple Controller: Switcher and 2 LDO Outputs
- Optimized for Pentium II* and AMD** K6-2 Processors
- 250 kHz. Switching Frequency
- Current Mode Operation with User Programmable Limit

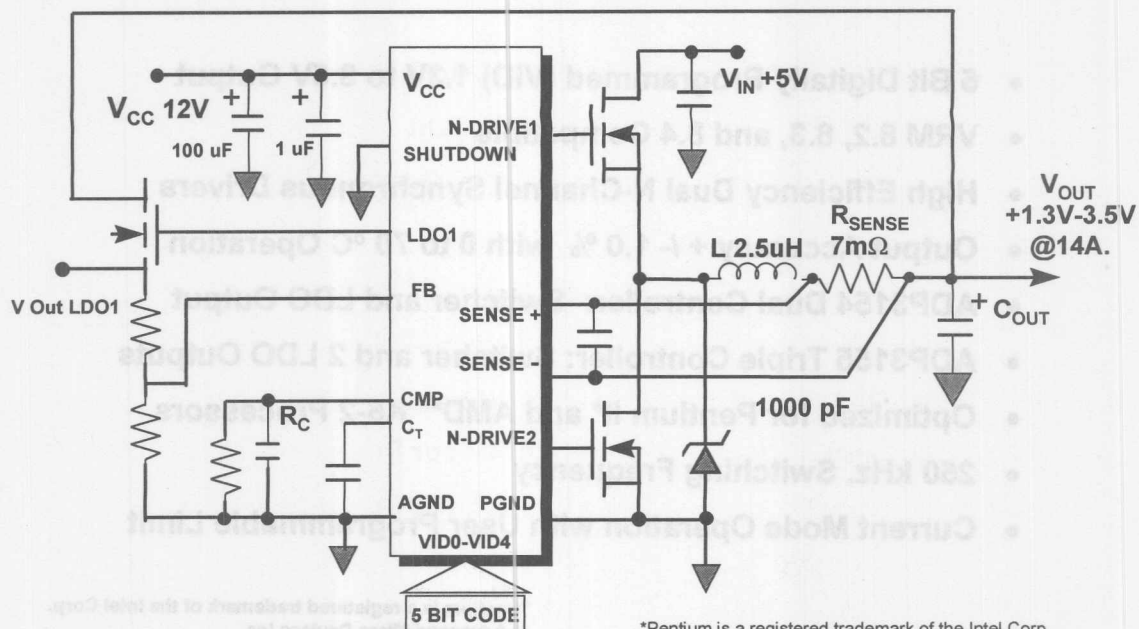
*Pentium is a registered trademark of the Intel Corp.

** Advanced Micro Devices Inc

8 - 29



ADP3154/ADP3155 5 Bit VID Programmable Dual, Triple Converter for Pentium II* Processors



*Pentium is a registered trademark of the Intel Corp.

8-30



ADP3156, ADP3157 **5 Bit VID Code Programmable** **Power Supply Controllers for the Pentium III* Processor**

- 5 Bit Digitally Programmed (VID) 1.3V to 3.5V Output
- VRM 8.2, VRM 8.3 and VRM 8.4 Compliant
- Active Voltage Positioning and Power Good Output
- High Efficiency, Current Mode Operation
- Output Accuracy $\pm 1.0\%$ with 0 to 70 °C Operation
- Optimized for Pentium III* and AMD** K6-2 Processors
- Up to 400 kHz. Programmable Switching Frequency
- Overvoltage Crowbar for Microprocessor Protection
- Short Circuit Protected and User Defined Current Limit
- SO-16 Package

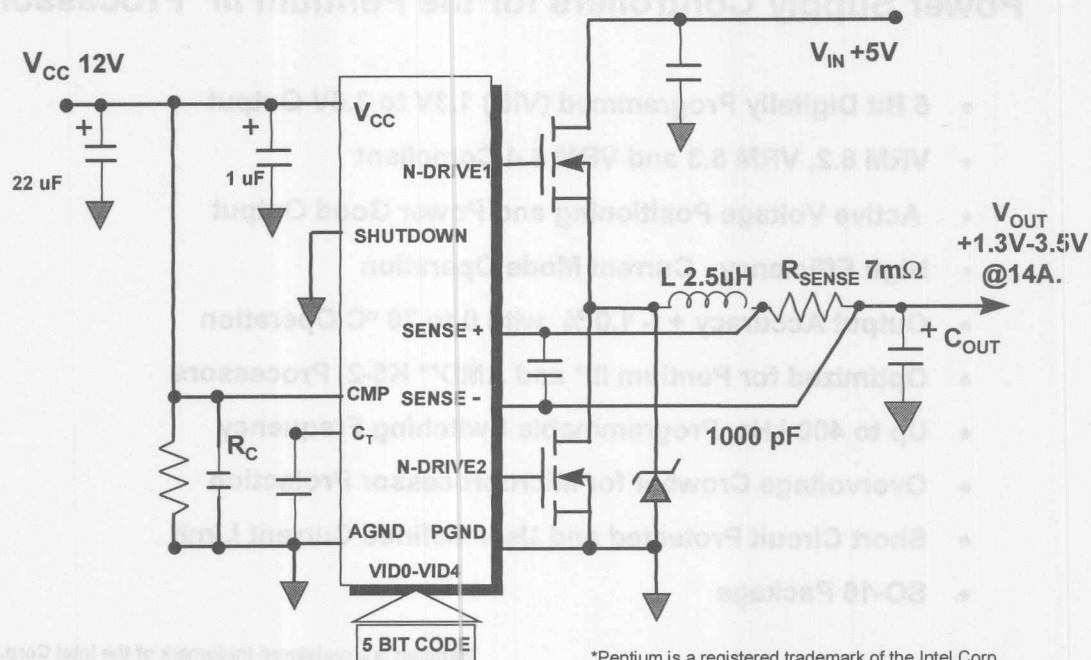
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** Advanced Micro Devices Inc

8 - 31



ADP3156/ADP3157 5 Bit VID Programmable Output Converter for Pentium II* Processors



*Pentium is a registered trademark of the Intel Corp.

8 - 32

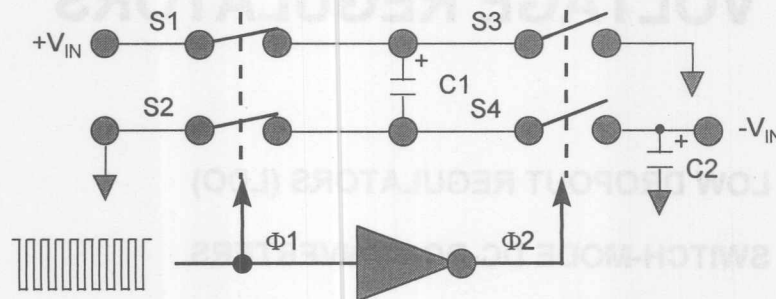


VOLTAGE REGULATORS

- LOW DROPOUT REGULATORS (LDO)
- SWITCH-MODE DC-DC CONVERTERS
- ➔ SWITCHED CAPACITOR VOLTAGE CONVERTER
- BATTERY CHARGER CONTROLLERS



A Switched Capacitor Voltage Inverter

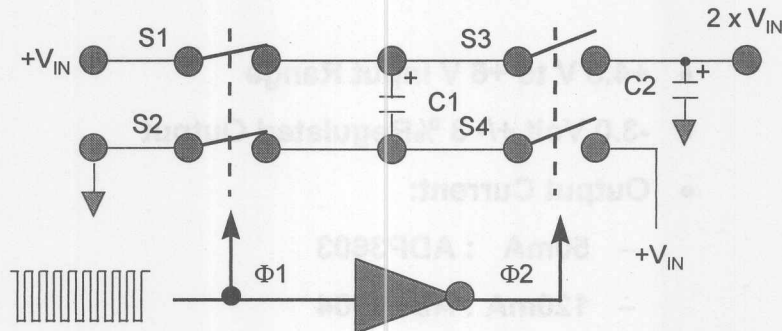


- When S1 and S2 are closed, and S3 and S4 Open, C1 Charges to $q1 = C1 \times V_{IN}$
- When S1 and S2 are Open, and S3 and S4 are Closed, The Charge on C1 is Transferred to C2 and Inverted

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A Switched Capacitor Voltage Doubler



- When S1 and S2 are closed, and S3 and S4 Open, C1 Charges to $q_1 = C_1 \times V_{IN}$
- When S1 and S2 are Open, and S3 and S4 are Closed, The Charge from C1 (q_1) plus an equal charge q_2 ($C_2 \times V_{IN}$;) is Transferred to C2. Since $q_1 = q_2$, $V_{OUT} = 2 \times V_{IN}$.

8 - 35



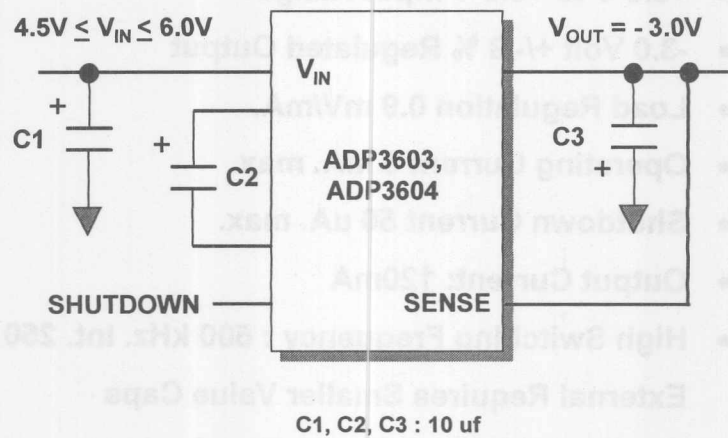
ADP3603 and ADP3604 Switched Capacitor Voltage Converters

- **+4.5 V to +6 V Input Range**
- **-3.0 Volt +/- 3 % Regulated Output**
- **Output Current:**
 - **50mA : ADP3603**
 - **120mA : ADP3604**
- **High Switching Frequency : 120kHz**
- **Shut-Down Pin**
- **Easy-to-Use, No Inductors Required**
- **8 Pin SOIC Package**

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ADP3603, ADP3604 - Application Example



8-37



ADP3605

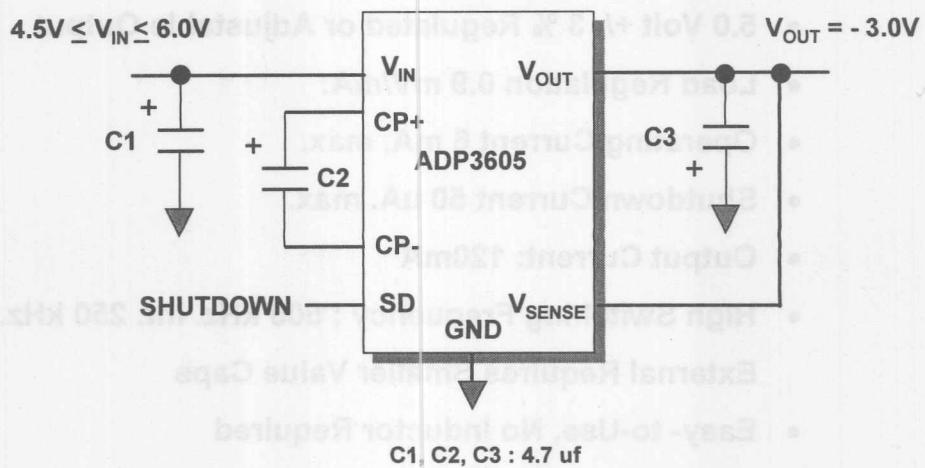
Switched Capacitor Voltage Converter

- **+3.0 V to +6.0 V Input Range**
- **-3.0 Volt +/- 3 % Regulated Output**
- **Load Regulation 0.9 mV/mA.**
- **Operating Current 6 mA. max.**
- **Shutdown Current 50 uA. max.**
- **Output Current: 120mA**
- **High Switching Frequency : 500 kHz. Int. 250 kHz.**
External Requires Smaller Value Caps
- **Easy- to-Use, No Inductor Required**
- **8 Pin SOIC and TSSOP Packages**
-

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ADP3605 - Application Example



8 - 39



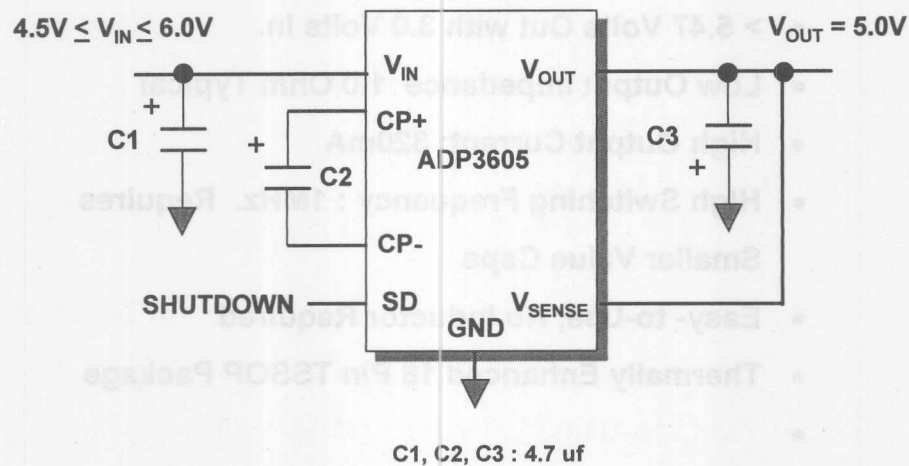
ADP3607 Switched Capacitor Regulated Voltage Boost

- **+3.0 V to +6.0 V Input Range**
- **5.0 Volt +/- 3 % Regulated or Adjustable Output**
- **Load Regulation 0.9 mV/mA.**
- **Operating Current 6 mA. max.**
- **Shutdown Current 50 uA. max.**
- **Output Current: 120mA**
- **High Switching Frequency : 500 kHz. Int. 250 kHz.**
External Requires Smaller Value Caps
- **Easy- to-Use, No Inductor Required**
- **8 Pin SOIC and TSSOP Packages**
-

8 - 40



ADP3607 - Application Example



8-41



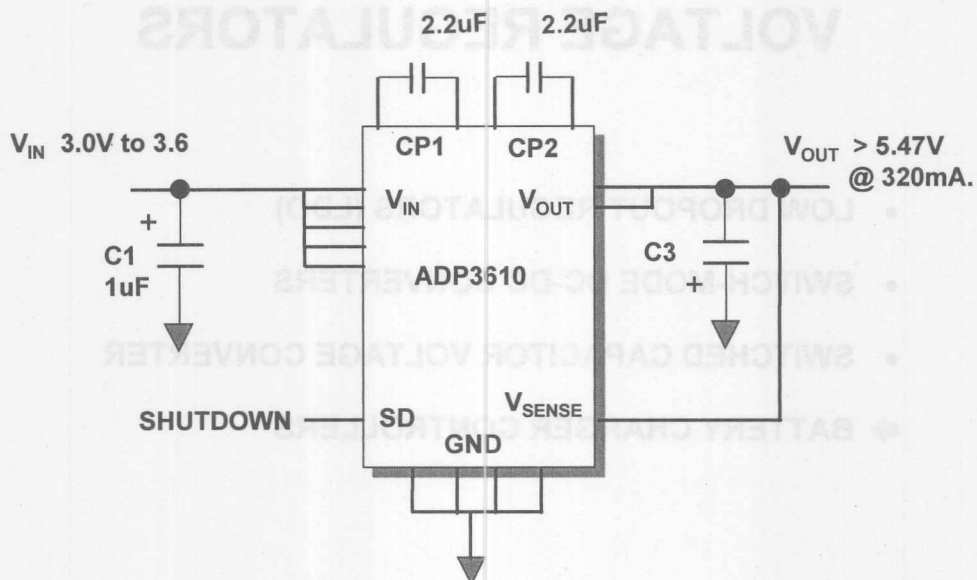
ADP3610 Switched Capacitor 320mA. Regulated Voltage Boost

- **+3.0 V to + 3.6 V Input Range**
- **> 5.47 Volts Out with 3.0 Volts In.**
- **Low Output Impedance 1.0 Ohm Typical**
- **High Output Current: 320mA**
- **High Switching Frequency : 1MHz. Requires Smaller Value Caps**
- **Easy- to-Use, No Inductor Required**
- **Thermally Enhanced 16 Pin TSSOP Package**
-

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ADP3610 - Application Example



8-43



VOLTAGE REGULATORS

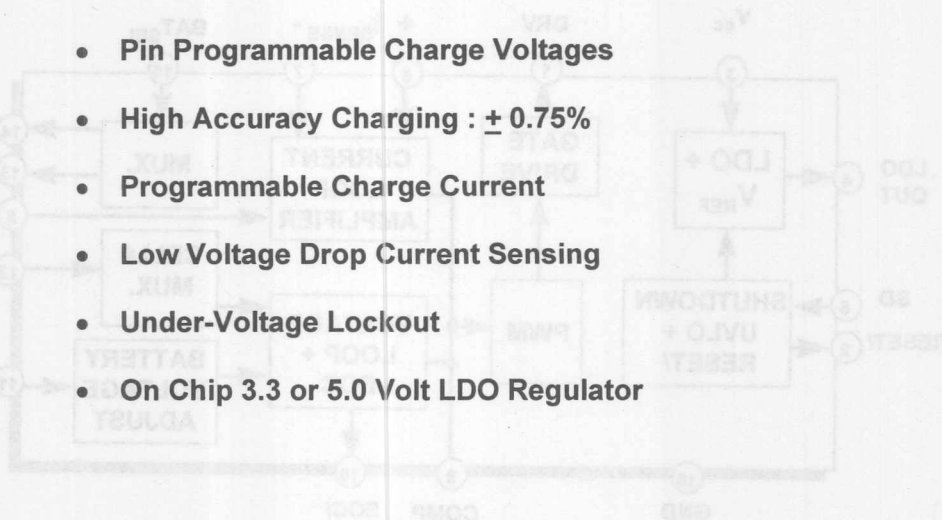
- LOW DROPOUT REGULATORS (LDO)
- SWITCH-MODE DC-DC CONVERTERS
- SWITCHED CAPACITOR VOLTAGE CONVERTER
- ➔ BATTERY CHARGER CONTROLLERS



Preliminary
Information

ADP3801 and ADP3802 Complete Dual Battery Charging ICs.

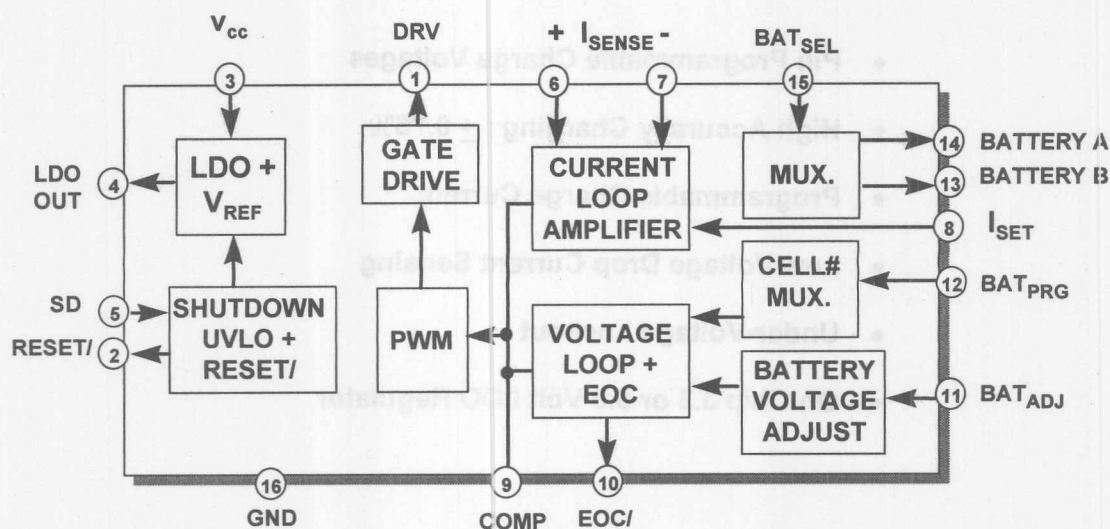
- Pin Programmable Charge Voltages
- High Accuracy Charging : $\pm 0.75\%$
- Programmable Charge Current
- Low Voltage Drop Current Sensing
- Under-Voltage Lockout
- On Chip 3.3 or 5.0 Volt LDO Regulator



8-45



ADP3801, ADP3802 **Dual Lithium - Ion, NiMH Battery Charger with Built** **In LDO**

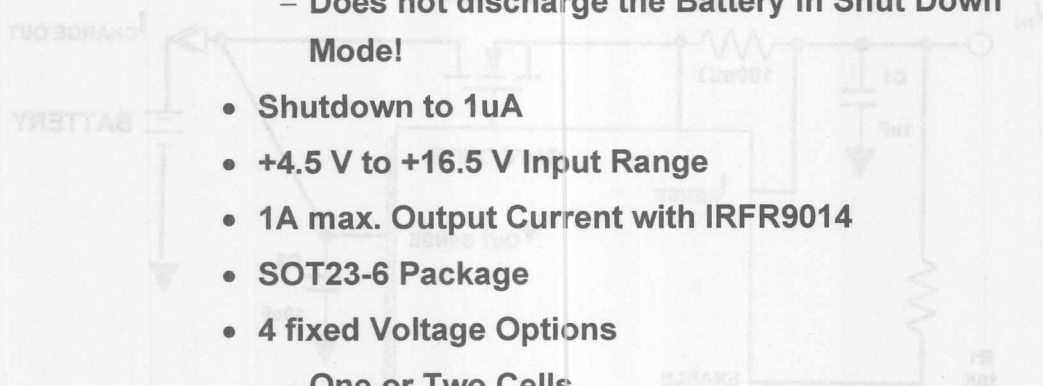


8-46



ADP3820

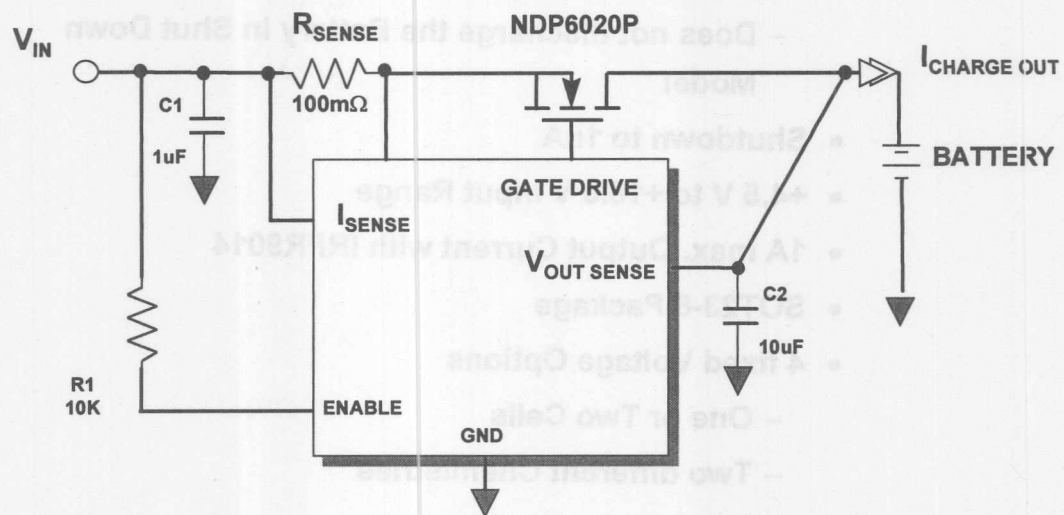
- 1% Accuracy
- Integrated Reverse Leakage Protection
 - Does not discharge the Battery in Shut Down Mode!
- Shutdown to 1uA
- +4.5 V to +16.5 V Input Range
- 1A max. Output Current with IRFR9014
- SOT23-6 Package
- 4 fixed Voltage Options
 - One or Two Cells
 - Two different Chemistries



8-47



ADP3820 Lithium-Ion Linear Battery Charger



8-48



Section 9

Microprocessor Supervisory Components

Power Supply Monitors
Supervisory Components
Hardware Monitoring System

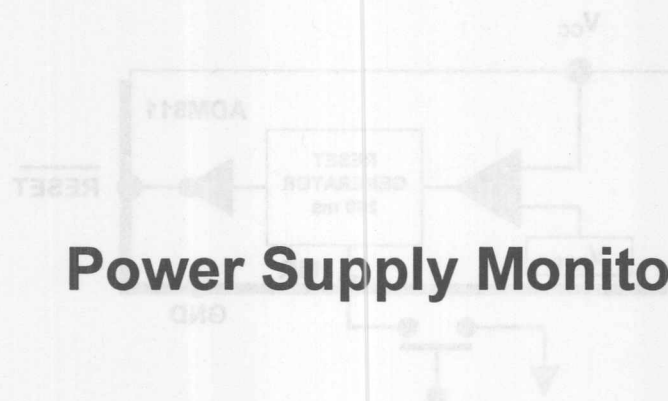


Section 9 Microprocessor Supervisory Components

Power Supply Monitors
Supervisory Components
Hardware Monitoring System



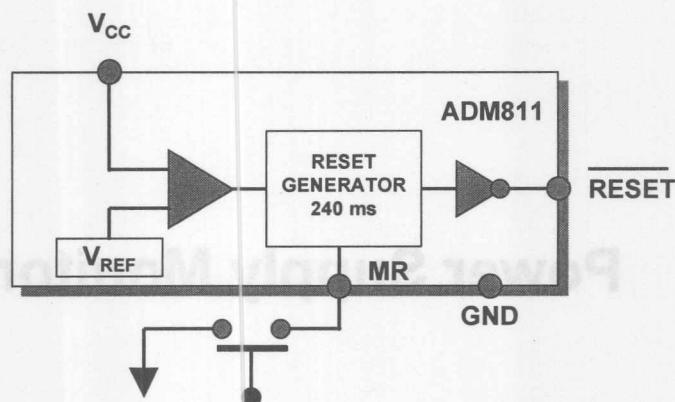
Power Supply Monitors



- Precision Voltage Monitor
- Manual RESET
- Logic Low RESET Output (ADM811)
- Logic High RESET Output (ADM812)
- Reset Assertion Down to 1 V_{cc}
- +3V, +2.3V and +5V Options
- Low Power Consumption: 8 nA
- 4 Pin SOT-143 Package



ADM811 and ADM812 V_{CC} Monitors



- Precision Voltage Monitor
- Manual RESET
- Logic Low RESET Output (ADM811)
- Logic High RESET Output (ADM812)
- Reset Assertion Down to 1 V V_{CC}
- + 3V, + 3.3V and + 5V Options
- Low Power Consumption : 6 μ A
- 4 Pin SOT-143 Package



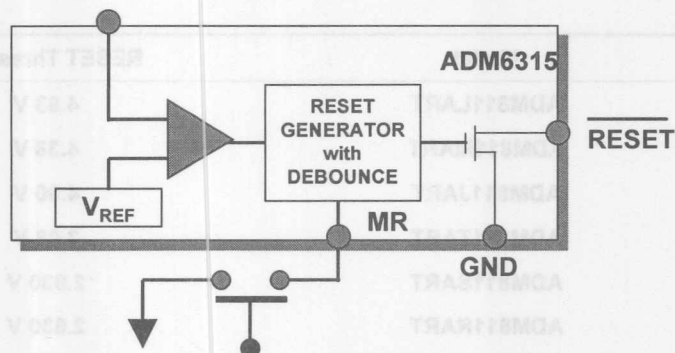
ADM811 and ADM812 Options

Model	RESET Threshold
ADM811LART	4.63 V
ADM811MART	4.38 V
ADM811JART	4.00 V
ADM811TART	3.08 V
ADM811SART	2.930 V
ADM811RART	2.630 V
ADM812LART	4.63 V
ADM812MART	4.38 V
ADM812JART	4.00 V
ADM812TART	3.08 V
ADM812SART	2.930 V
ADM812RART	2.630 V



Preliminary
Information

ADM6315 V_{CC} Monitor



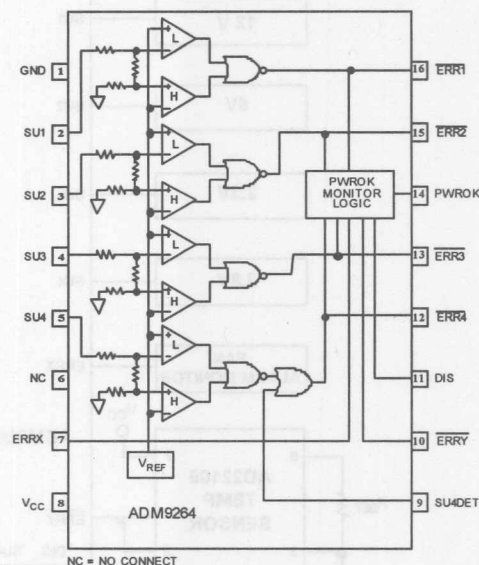
- Precision Voltage Monitor
- 5 μ A Supply Current
- SOT143 Package
- Four Reset Timeout Options :1ms, 20ms, 140ms, 1120ms
- Open Drain RESET Output
- Upgrade for MAX6315
- 9 Pin MicroSOIC Package



ADM9268 Quad Supply Monitor

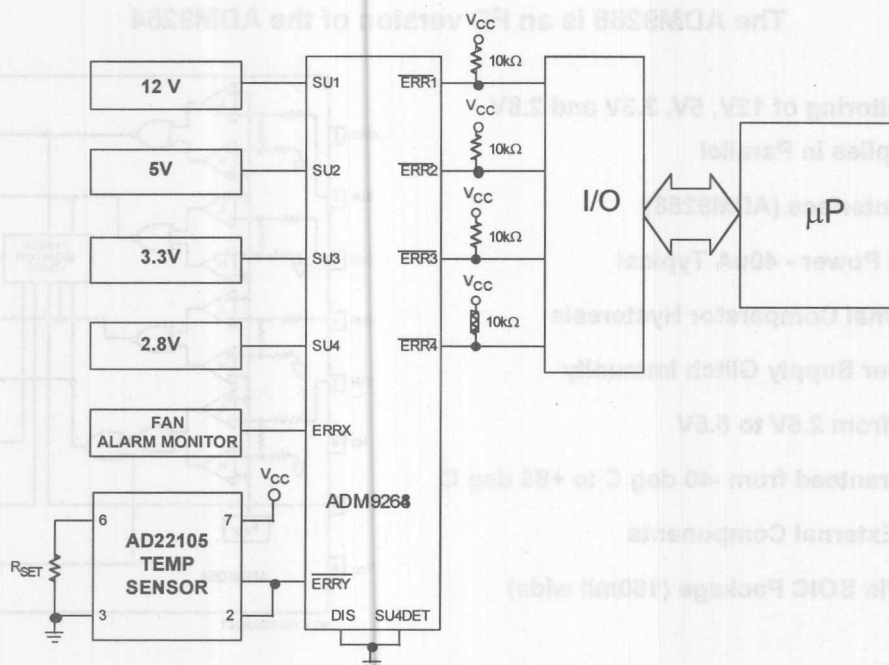
The ADM9268 is an I²C version of the ADM9264

- Monitoring of 12V, 5V, 3.3V and 2.8V Supplies in Parallel
- I²C Interface (ADM9268)
- Low Power - 40uA Typical
- Internal Comparator Hysteresis
- Power Supply Glitch Immunity
- V_{CC} from 2.5V to 5.5V
- Guaranteed from -40 deg C to +85 deg C
- No External Components
- 16 Pin SOIC Package (150mil wide)





ADM9268 Multi-Supply Monitoring



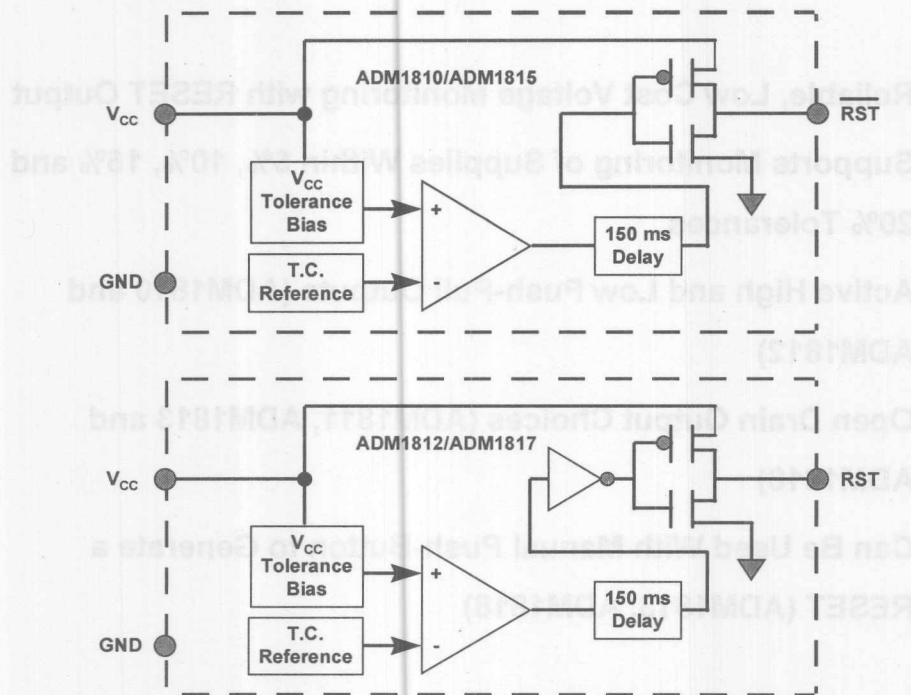


ADM181X Family Low Cost Microprocessor Reset Circuits

- **Reliable, Low Cost Voltage Monitoring with RESET Output**
- **Supports Monitoring of Supplies Within 5%, 10%, 15% and 20% Tolerances**
- **Active High and Low Push-Pull Outputs (ADM1810 and ADM1812)**
- **Open Drain Output Choices (ADM1811, ADM1813 and ADM1818)**
- **Can Be Used With Manual Push-Button to Generate a RESET (ADM1813, ADM1818)**

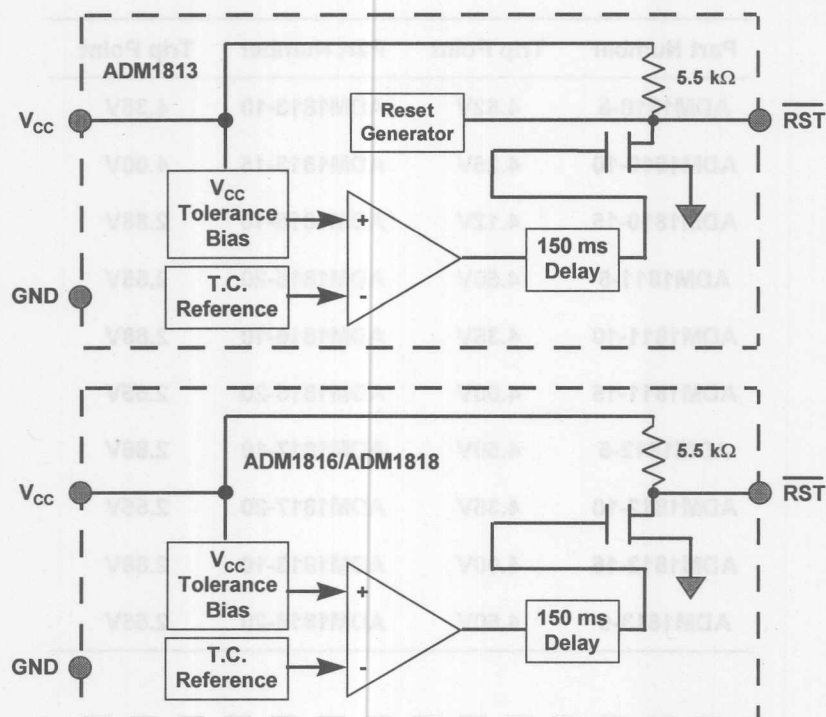


ADM181X - Block Diagrams





ADM181X - Block Diagrams (con't)





ADM181X Ordering Guide

Part Number	Trip Point	Part Number	Trip Point
ADM1810-5	4.62V	ADM1813-10	4.35V
ADM1810-10	4.25V	ADM1813-15	4.00V
ADM1810-15	4.12V	ADM1815-10	2.88V
ADM1811-5	4.50V	ADM1815-20	2.55V
ADM1811-10	4.35V	ADM1816-10	2.88V
ADM1811-15	4.00V	ADM1816-20	2.55V
ADM1812-5	4.50V	ADM1817-10	2.88V
ADM1812-10	4.35V	ADM1817-20	2.55V
ADM1812-15	4.00V	ADM1818-10	2.88V
ADM1813-5	4.50V	ADM1818-20	2.55V



Hardware Monitoring System



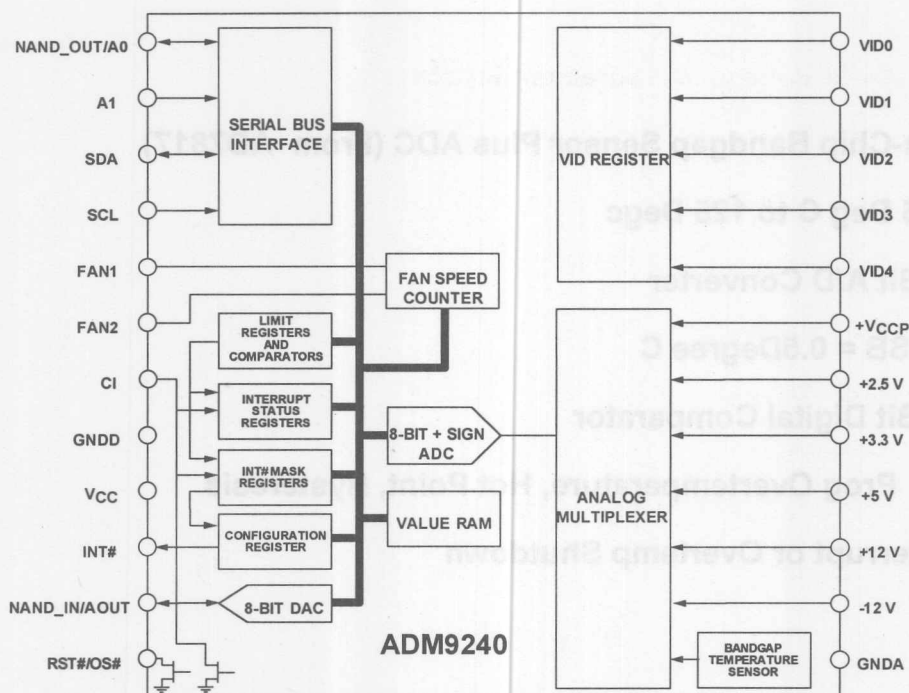
ADM9240

ADC Based System Hardware Monitor

- **6 Direct Voltage Measurement Inputs**
- **On-Chip Temperature Sensor**
- **Limit Comparison of all Monitored Values**
- **5 Digital Inputs for VID Bits**
- **2 Fan Speed Monitoring Inputs**
- **Chassis Intrusion Detect**
- **LDCM Support**
- **I²C Compatible Serial Bus Interface**
- **Programmable Reset/Overtemperature Shutdown Pin**
- **Shutdown Mode to Minimize Power Consumption**



ADM9240 Functional Block Diagram





On-Chip Temperature Measurement

- On-Chip Bandgap Sensor Plus ADC (From AD7817)
- -55 Deg C to 125 Degc
- 9 Bit A/D Converter
- 1LSB = 0.5Degree C
- 8-Bit Digital Comparator
 - Prog Overtemperature, Hot Point, Hysteresis
- Interrupt or Overtemp Shutdown



VID Monitoring

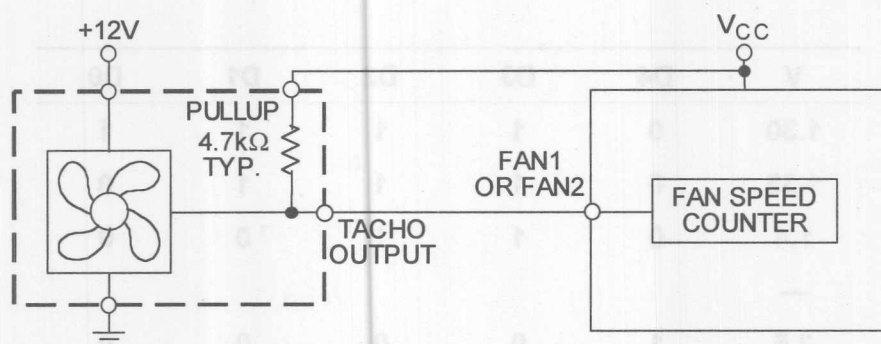
V	D4	D3	D2	D1	D0
1.30	0	1	1	1	1
1.35	0	1	1	1	0
1.4	0	1	1	0	0

3.5	1	0	0	0	0

- 5-Bit Voltage -ID Code From Klamath CPU
- Gives Optimum Voltage Required by Core Logic
- Depends on Probe Yield, Clock Speed



Fan Tachometer Input



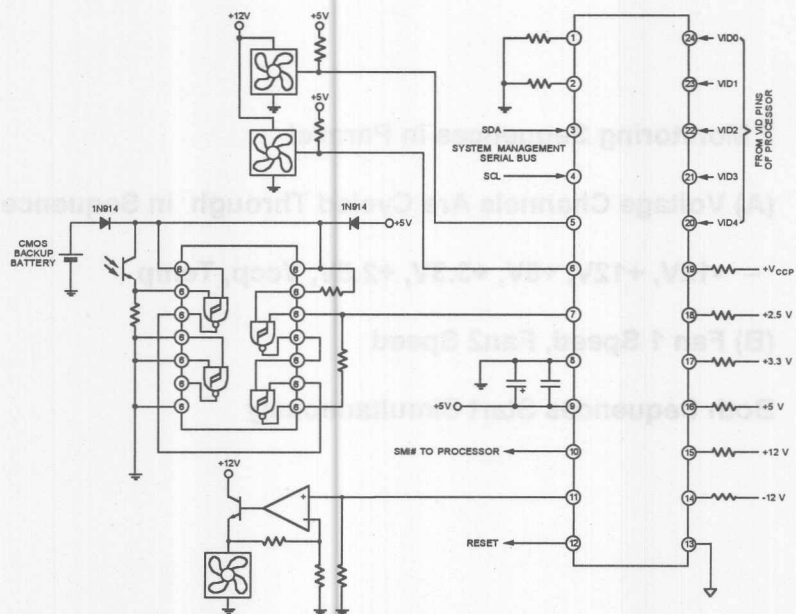
- Two Tacho Inputs
 - Tacho gives two pulses per revolution
 - Hysteresis to accommodate slow rise/fall time
- Tacho gates internal 22.5kHz Oscillator for one period.



Monitoring Sequence

- **2 Monitoring Sequences in Parallel**
- **(A) Voltage Channels Are Cycled Through in Sequence**
 - **-12V, +12V, +5V, +3.3V, +2.5V, Vccp, Temp**
- **(B) Fan 1 Speed, Fan2 Speed**
- **Both Sequences Start Simultaneously**

Typical Application





ADM1021 Microprocessor Temperature Monitor

The ADM1021 is a low cost, two-channel digital thermometer and under/over temperature alarm, intended for use in personal computers and other systems requiring thermal monitoring and management.



ADM1021 - Key Specs and Features

- **Improved Replacement for MAX1617**
- **On-Chip and Remote Temperature Sensing - No Calibration Necessary**
- **High Accuracy :**
 - **± 1 deg C typ (On-Chip Sensor)**
 - **± 3 deg C max (Remote Sensor)**
- **Programmable Over/Under Temperature Limits**
- **Programmable Conversion Rates**



ADM1021 - Key Specs and Features (con't)

- **2-Wire System Management Bus (SMBus™) Serial Interface**
- **Supports SMBus™ Alert**
- **Single Supply, Low Power Operation :**
 - **+ 3V to + 5.5V Supply**
 - **70 uA Max Quiescent Current**
 - **3 uA Standby Current**
- **Small 16 Lead QSOP Package**



ADM1021 - Key Specs and Features (con't)

- 2-Wire System Management Bus (SMBus™) Serial Interface
- Supports SMBus™ Alert
- Single Supply, Low Power Operation:
 - +3V to +5.5V Supply
 - 70 μ A Max Quiescent Current
 - 3 μ A Standby Current
- Small 16 Lead QSO-P Package



SECTION 10

AUDIO PRODUCTS

Power and Precision Audio Amplifiers

Surround Sound System

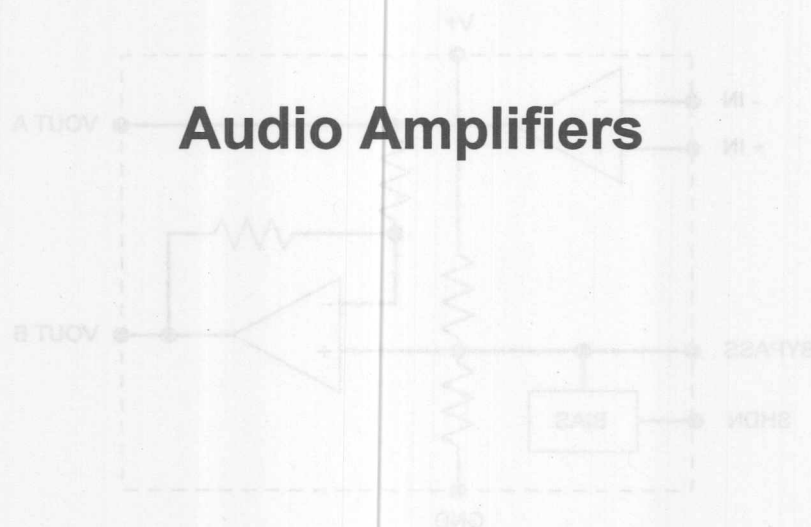


SECTION 10 AUDIO PRODUCTS

Surround Sound System
Power and Precision Audio Amplifiers



Audio Amplifiers

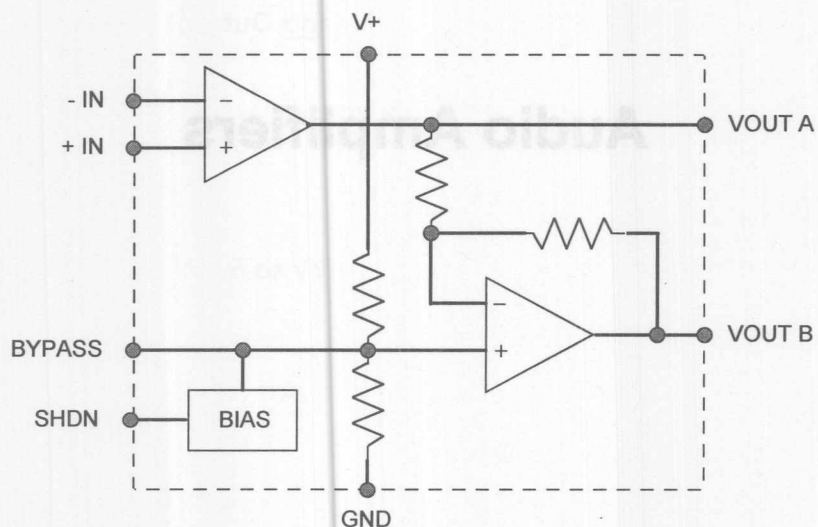




SSM2211

1 Watt Audio Power Amplifier

Amazing! One watt of power into 8 ohms at less than 1 % THD in an 8 lead, narrow body SOIC package!



10-4



SSM2211 - Key Specs and Features

- **Proprietary new Thermal Coastline™ 8 lead SOIC package**
- **Differential Rail-Rail Inputs and Outputs**
- **4 MHz Bandwidth**
- **Low Distortion (into 8 ohms):**
 - **< 0.4% @ 1W**
- **Single Supply Operation : 2.7V to 5.5V**
- **Supply current only 3.5mA**
 - **SHUTDOWN Mode < 100 nA**
- **-40 deg C to + 85 deg C**

10 - 5



SSM2275 and SSM2475 Dual/Quad *Rail-Rail* Audio Amplifiers

The SSM2275 and SSM2475 are dual and quad rail-rail versions of our popular OP275 Audio amplifier

- Rail-Rail Outputs
- Unity Gain Bandwidth : 8 MHz
- Slew Rate :11V/us
- Total Harmonic Distortion < 0.004%
- Noise Density < 7 nV/root Hz
- Single (+ 5V) or Dual (\pm 15V) Supply Operation
- Low Supply Current : 3 mA/Amplifier
- - 40 deg C to + 85 deg C
- 8/14 Pin DIP, SOIC and TSSOP Packages

10 - 6



Surround Sound System



Analog Devices' New Circle Surround® Audio Sound System...

**The Most Exciting Development in Audio
Entertainment Since the Advent of
Surround Sound Technology!**



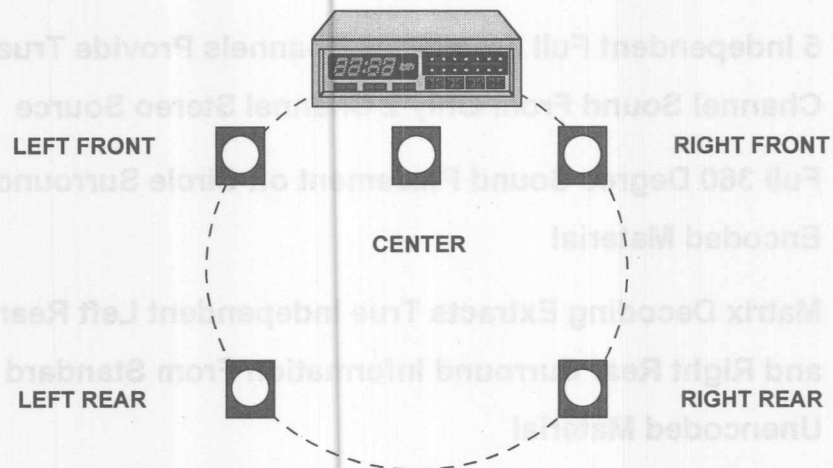
**PRELIMINARY
INFORMATION**

SSM2005 Circle Surround® Audio Surround System

- **5 Independent Full Frequency Channels Provide True 5 Channel Sound From Only 2 Channel Stereo Source**
- **Full 360 Degree Sound Placement on Circle Surround Encoded Material**
- **Matrix Decoding Extracts True Independent Left Rear and Right Rear Surround Information From Standard Unencoded Material**
- **Enhanced Playback of Dolby Prologic® Encoded Material**



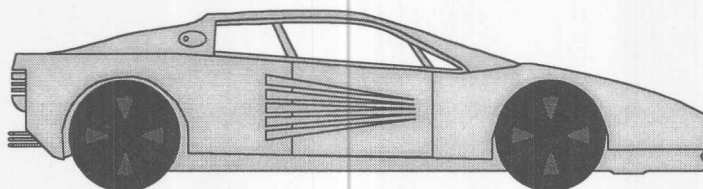
Superior Sound for Home Theater and Music Systems...



- **5 Independent Channels for 360 Degree Placement**
- **Full Bandwidth At All Channels for Balanced Sound**
- **Superior Decoding of Prologic® Material**



Superior Sound for Autosound...



- **Full Bandwidth in Rear Speakers**
- **Every Seat is a Good Seat - Excellent Separation**
- **Surround Sound from AM, FM, Tape and CD!**



Superior Sound for Autosound...



- Full Bandwidth in Rear Speakers
- Every Seat is a Good Seat - Excellent Separation
- Ground Sound from AM, FM, Tape and CD!



SECTION 11 MONOLITHIC SENSOR PRODUCTS

Temperature Sensors/Controllers

Sensor Signal Conditioners

Monolithic Accelerometers



SECTION 11 MONOLITHIC SENSOR PRODUCTS

Temperature Sensor Controllers
Sensor Signal Conditioners
Monolithic Accelerometers



Temperature Sensors



Current Output

Voltage Output

Digital Output

Temperature Controllers



AD590, AD592 and TMP17 Low Cost, Current Output Temperature Sensors

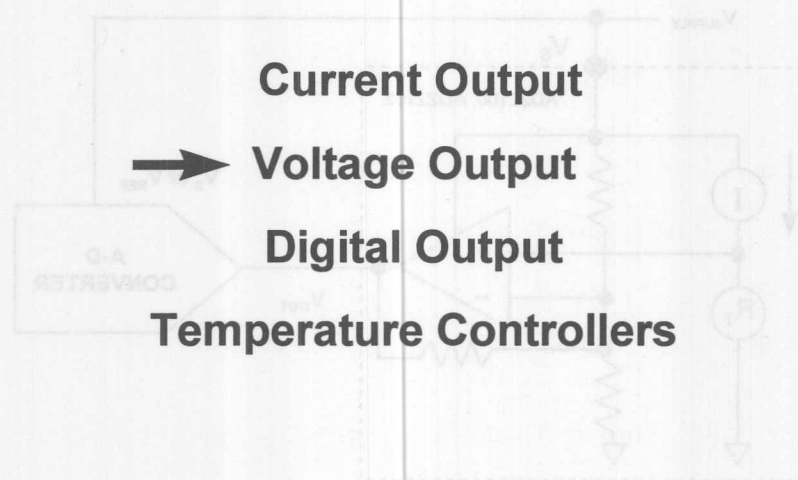
The AD590, AD592 and TMP17 produce a linear output current proportional to temperature

	AD590	AD592	TMP17
Basic Accuracy	± 0.5 deg C	± 0.5 deg C	± 2.5 deg C
Temp Range	-55 C to +150 C	-40 C to +105 C	-25 C to +105 C
Current Output @ + 25 deg C	298.2 uA	298.2 uA	298.2 uA
Tempco	1 uA/deg K	1 uA/deg C	1 uA/deg C
Supply Voltage	+4V to +30V	+4V to +30V	+4V to +30V
Package Styles	TO-52 Can, 2 Lead Flatpack	TO-92	8 Pin SOIC
Comment	Highest Accuracy	High Accuracy	Lowest Cost

11-4



Temperature Sensors



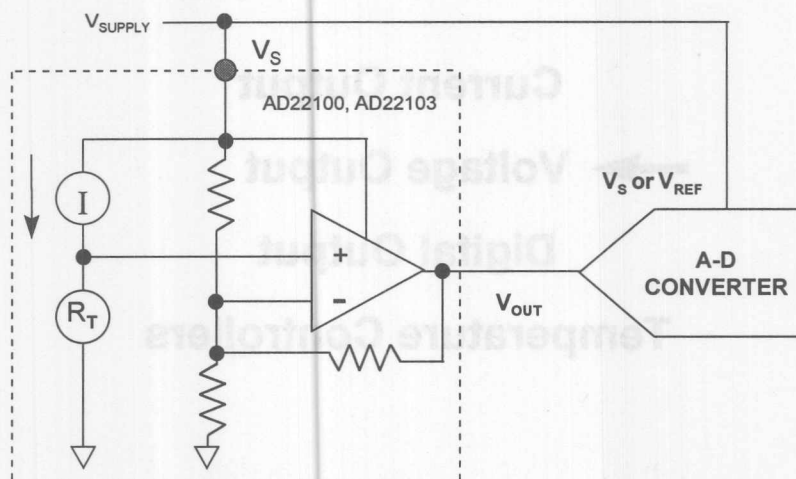
Temperature Controllers

11-5



AD22100 and AD22103 Monolithic Temperature Sensors

The AD22100 and AD22103 are low cost, single supply temperature sensor ICs whose output voltages are directly proportional to temperature.



11-6



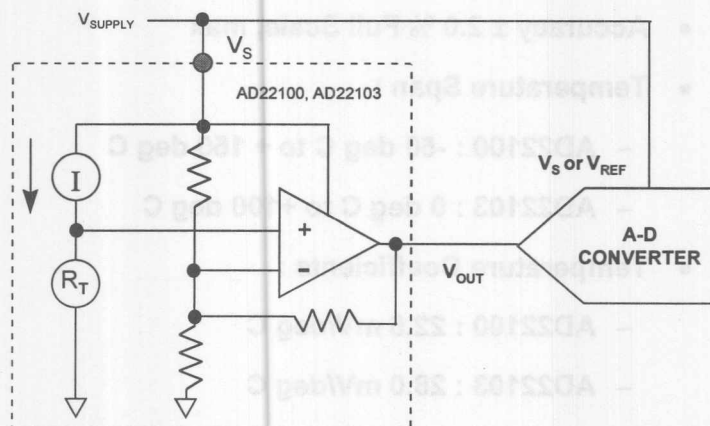
AD22100, AD22103 - Key Specs and Features

- **Accuracy $\pm 2.0\%$ Full Scale, max**
- **Temperature Span :**
 - **AD22100 : -50 deg C to + 150 deg C**
 - **AD22103 : 0 deg C to +100 deg C**
- **Temperature Coefficients :**
 - **AD22100 : 22.5 mV/deg C**
 - **AD22103 : 28.0 mV/deg C**
- **Low Power, Single Supply Operation:**
 - **AD22100 : + 5V @ 650 uA max**
 - **AD22103 : + 3V @ 600 uA max**
- **Reverse Supply Voltage Protection**

11 - 7



The AD22100/22103's Output is Ratiometric to the Power Supply...no Precision Source is Necessary!



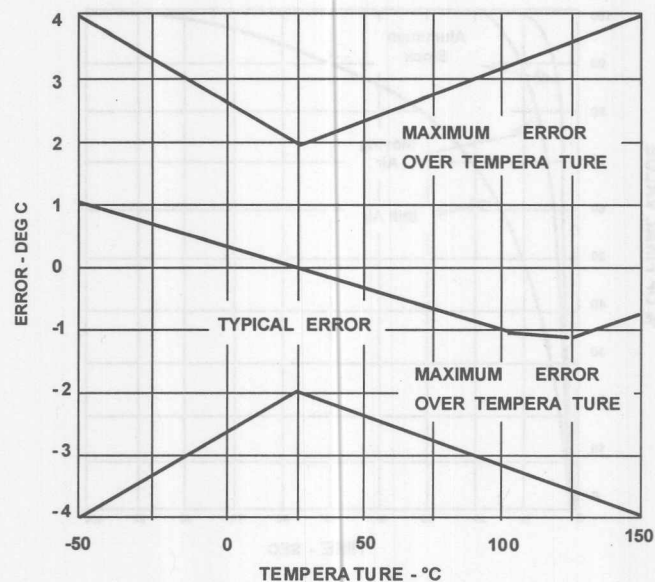
$$\text{AD22100: } V_{OUT} = \frac{V+}{5V} \times [1.375V + (22.5 \text{ mV/deg C} \times T_{AMB})]$$

$$\text{AD22103: } V_{OUT} = \frac{V+}{3.3V} \times [0.25V + (28.0 \text{ mV/deg C} \times T_{AMB})]$$

11 - 8



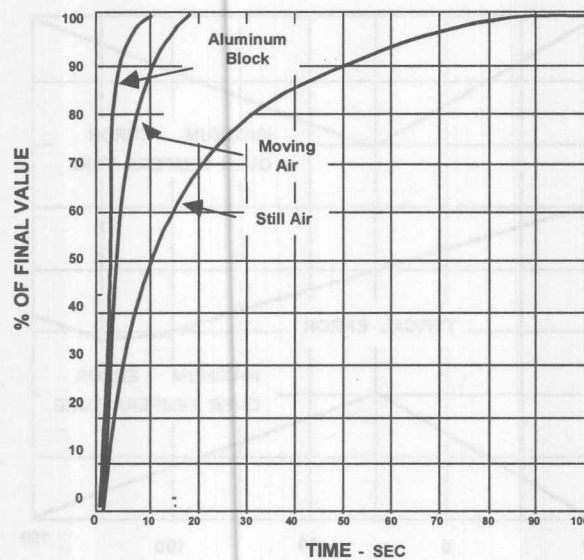
AD22100 - Typical Performance



11-9



AD22100 - Typical Response Time

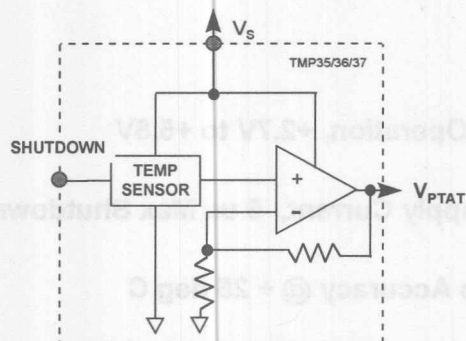


Response Time of the AD22100 for Various Mediums

11 - 10



TMP-35, TMP-36 and TMP-37 Low Cost, 3V Temperature Sensors



	TMP35	TMP36	TMP37
Temp Measurement Range	+ 10 C to + 125 C	- 40 C to + 125 C	+ 5 C to + 100 C
Output @ 25 deg C	250 mV	750 mV	500 mV
Scale Factor	10 mV/deg C	10 mV/deg C	20 mV/deg C
Compatible With	LM35/LM45	NA	LM50

11-11



TMP-35, TMP-36 and TMP-37 Key Specs and Features

- **Low-Voltage Operation, +2.7V to +5.5V**
- **50 μ A Max Supply Current, 5 μ A Max Shutdown Current**
- **± 1 deg C Typ Accuracy @ + 25 deg C**
- **$\pm 2^\circ\text{C}$ Typ Accuracy Over Temperature**
- **Less Than 0.1 deg C Error Due to Self-Heating**
- **-40°C to $+125^\circ\text{C}$ Operating Temperature Range**
- **8 Pin SOIC, 5 Pin SOT-23 and 3 Pin TO-92 Package Options**

11 - 12



Temperature Sensors

Current Output

Voltage Output



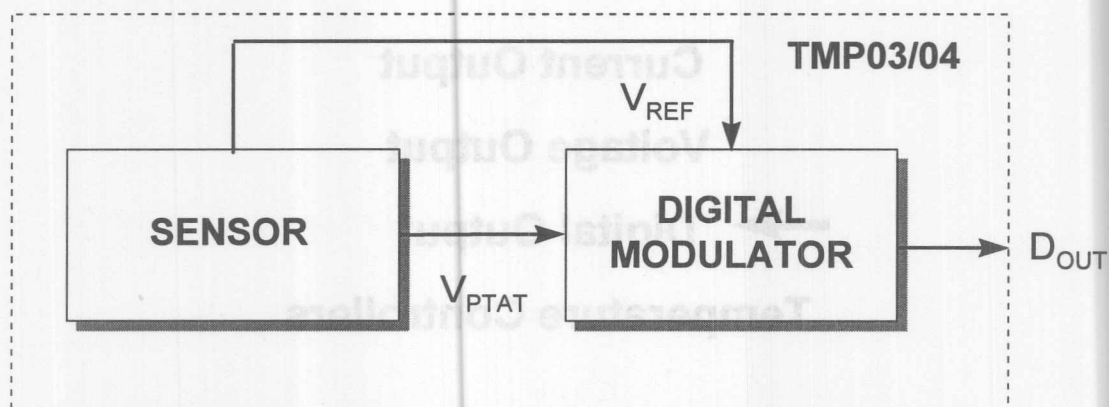
Digital Output

Temperature Controllers



TMP03 and TMP04 Micropower Temperature Sensors w/Serial Digital Outputs

The TMP03 and TMP04 are very low cost temperature sensors that produce an accurate, serial digital output whose duty cycle is proportional to temperature.



11 - 14

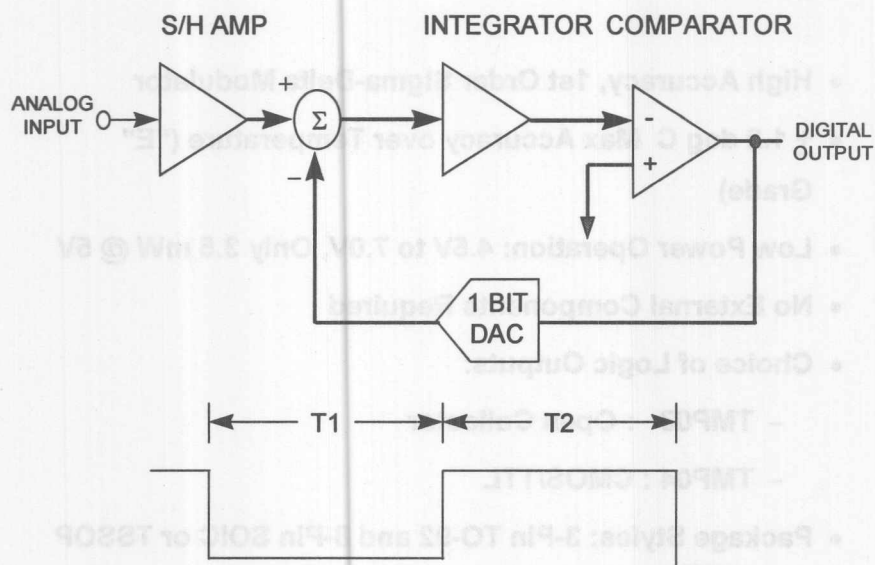


TMP03 and TMP04 - Key Specs and Features

- **High Accuracy, 1st Order Sigma-Delta Modulator**
- **± 1.2 deg C Max Accuracy over Temperature (“E” Grade)**
- **Low Power Operation: 4.5V to 7.0V, Only 3.5 mW @ 5V**
- **No External Components Required**
- **Choice of Logic Outputs:**
 - **TMP03 : Open Collector**
 - **TMP04 : CMOS/TTL**
- **Package Styles: 3-Pin TO-92 and 8-Pin SOIC or TSSOP**



Serial Digital Output Format



$$\text{Temp} = 260 - \frac{(450 \times T_1)}{T_2} ; \text{deg C}$$

11-16



AD7816, AD7817 and AD7818 1/4-Channel 10-Bit ADCs w/ On-Board Temp Sensor

- **100 ksps Throughput**
- **Input Channels :**
 - **AD7817 : 4 Channel**
 - **AD7818 : 1 Channel**
 - **AD7816 : Temp Sensor, Only**
- **On-Chip Temp Sensor :**
 - **0.25 deg C Resolution**
 - **± 1 deg C Error from -40 deg C to + 80 deg C**
 - **± 2 deg C Error from -55 deg C to + 125 deg C**

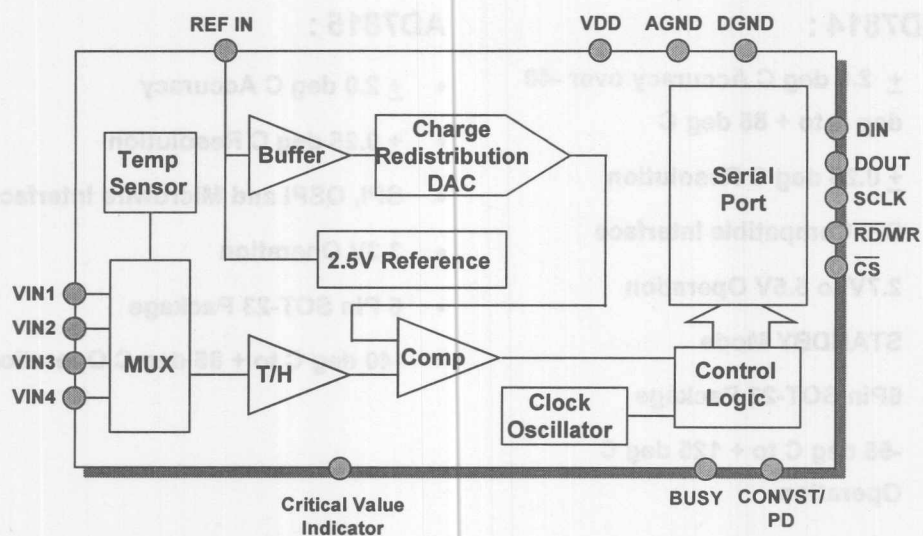


AD7816, AD7817 and AD7818 (con't)

- **On-Chip 2.5V Reference, $\pm 1\%$**
- **“Over Temperature” Indicator**
- **Low Power Performance :**
 - **560 μ W @ 50 ksps Throughput**
 - **Sleep Mode : 3 μ W max**
- **Flexible DSP/Microcontroller Serial Interface**
- **Power Down Mode W/ Data Readout During Powerdown**
- **Package Styles :**
 - **AD7817 : 16 Pin SOIC and TSSOP**
 - **AD7816, AD7818 : 8 Pin SOIC and MicroSOIC**



AD7817 - Block Diagram



11-19



Preliminary
Information

AD7814* and AD7815* 10 Bit Digital Temperature Sensors

AD7814 :

- ± 2.0 deg C Accuracy over -40 deg C to + 85 deg C
- ± 0.25 deg C Resolution
- SPI Compatible Interface
- 2.7V to 5.5V Operation
- STANDBY Mode
- 6Pin SOT-23 Package
- -55 deg C to + 125 deg C Operation

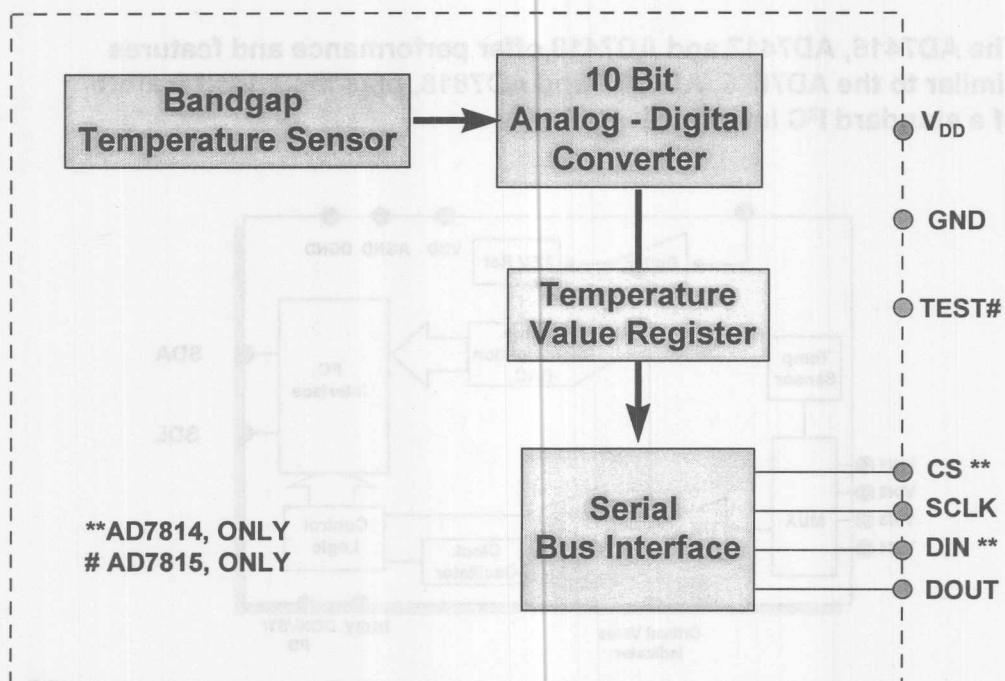
AD7815 :

- ± 2.0 deg C Accuracy
- ± 0.25 deg C Resolution
- SPI, QSPI and Microwire Interface
- 3.3V Operation
- 5 Pin SOT-23 Package
- -40 deg C to + 85 deg C Operation

11 - 20



AD7814, AD7815 - Simplified Diagram



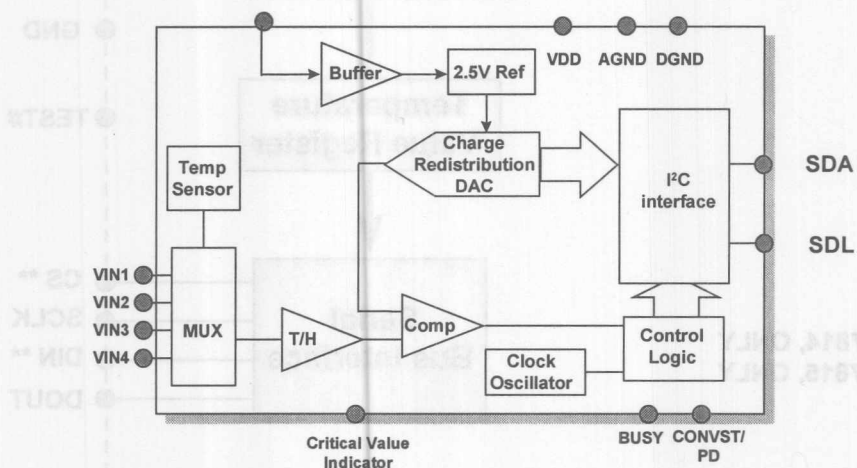
11 - 21



Preliminary
Information

AD7416, AD7417* and AD7418* 1/4-Channel 10-Bit ADCs w/ On-Board Temp Sensor

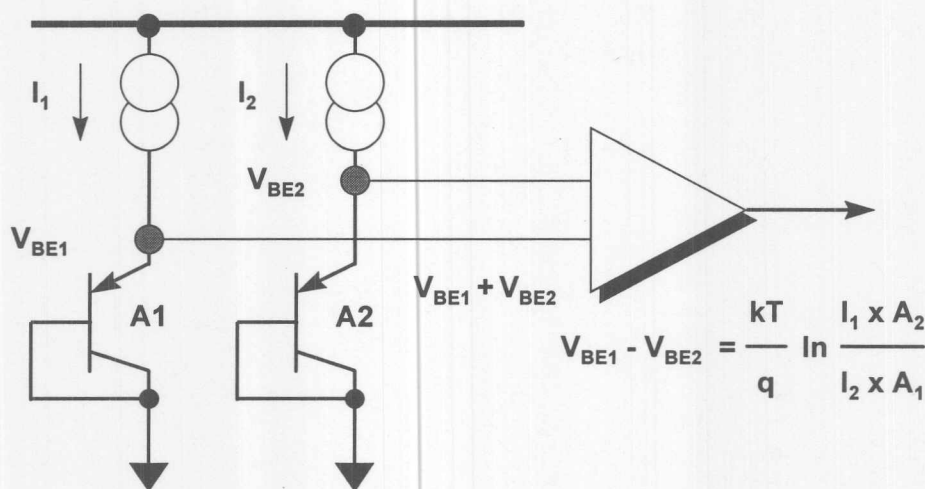
The AD7416, AD7417 and AD7418 offer performance and features similar to the AD7816, AD7817 and AD7818, plus the added feature of a standard I²C Interface



11 - 22



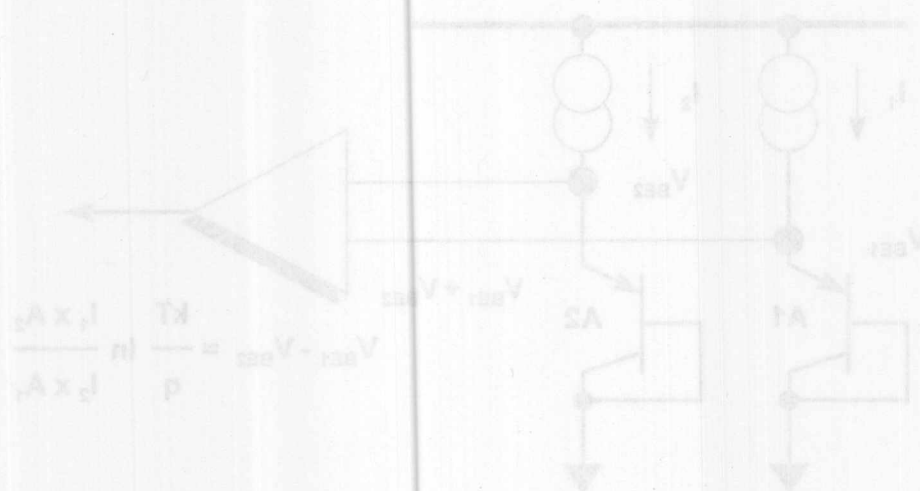
The On-Chip Temperature Sensor



11 - 23



The On-Chip Temperature Sensor



11 - 24



Temperature Sensors

Current Output

Voltage Output

Digital Output

→ Temperature Controllers

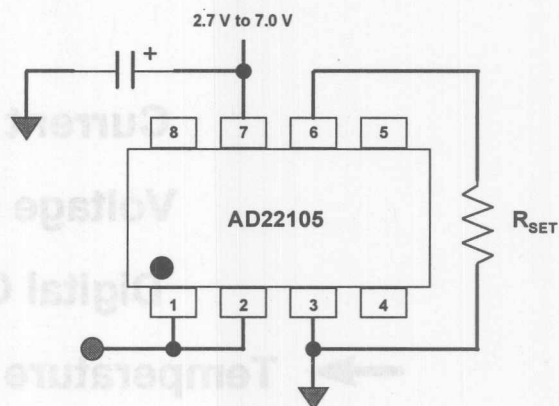
11 - 25



AD22105 Resistor Programmable Thermostat

The AD22105 is a low cost, reliable alternative to traditional electro-mechanical thermostatic switches.

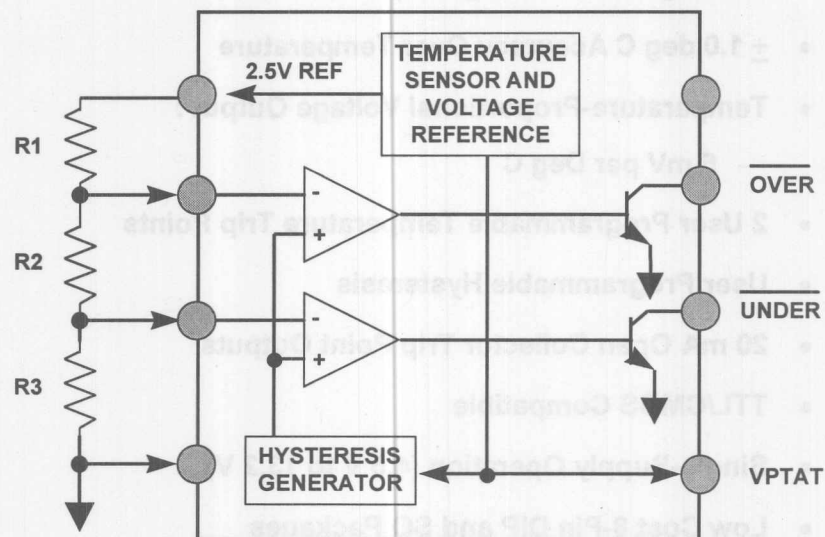
- Resistor-Programmable Setpoint
- 2.0 deg Setpoint Accuracy
- 4.0 deg Preset Hysteresis
- Open Collector Output
- Internal 200 k Ω Pull Up Resistor
- - 40 deg C to 150 deg C Range
- 2.7 V to 7.0 V Supply Range
- Low Power : 230 uW @ 3.3 V
- 8 Lead SOIC Package



11 - 26



TMP01 Low Power Temperature Controller



11 - 27



TMP01 - Key Specs and Features

- **-55 deg C to +125 deg C Operation**
- **± 1.0 deg C Accuracy Over Temperature**
- **Temperature-Proportional Voltage Output :**
 - **5 mV per Deg C**
- **2 User Programmable Temperature Trip Points**
- **User Programmable Hysteresis**
- **20 mA Open Collector Trip Point Outputs**
- **TTL/CMOS Compatible**
- **Single-Supply Operation (4.5 V to 13.2 V)**
- **Low Cost 8-Pin DIP and SO Packages**
- **Free Demo Software Calculates R Values!**

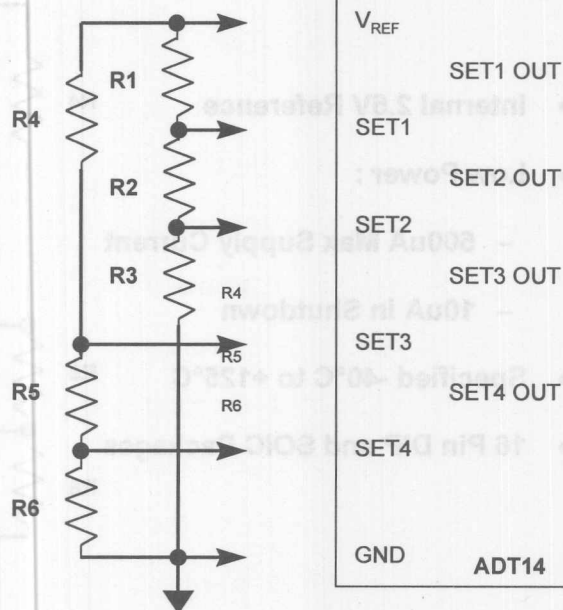
11 - 28



ADT14

Quad Setpoint, Programmable Temperature Monitor/Controller

- 5V Operation
- Four Resistor-Programmable Temperature Setpoints
- Programmable Hysteresis
- $\pm 3^{\circ}\text{C}$ Max Accuracy @ 25 deg C
- Linear V_{PTAT} Output, $+5\text{mV}/^{\circ}\text{C}$
- 5 mA Open-Collector Outputs

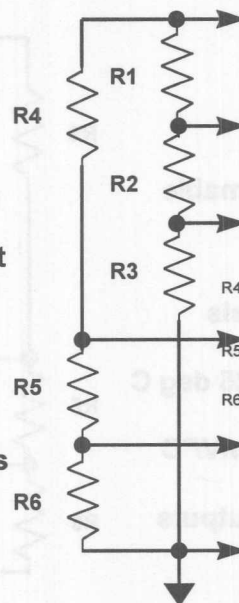


11 - 29



ADT14 (con't)

- Internal 2.5V Reference
- Low Power :
 - 500uA Max Supply Current
 - 10uA in Shutdown
- Specified -40°C to +125°C
- 16 Pin DIP and SOIC Packages



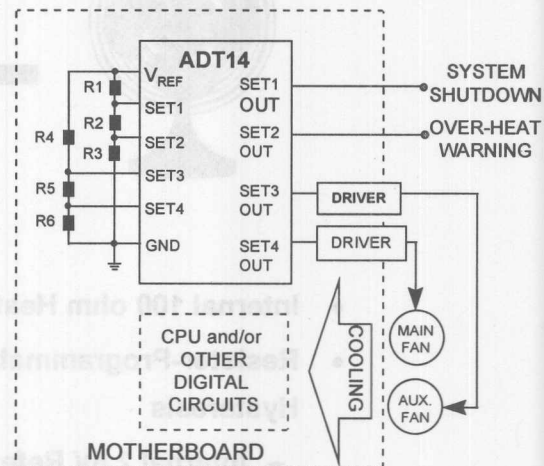
V_{REF}	
SET1 OUT	
SET1	
SET2 OUT	
SET2	
SET3 OUT	
SET3	
SET4 OUT	
SET4	
GND	ADT14

11 - 30



Example of Cooling Monitor in Server Application:

- Turn on Cooling Fan
- Increase Fan Speed or Turn on Auxiliary Fan
- Increase in Fan Speed Didn't Help... Send Warning Message to Operating System of Impending Shutdown.
- Temp Is Still Rising...Send Shutdown Signal to Power Supply.

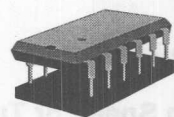
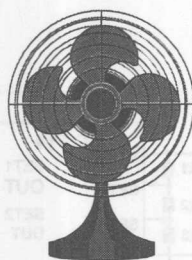


11 - 31



TMP-12

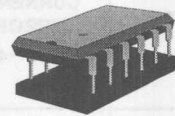
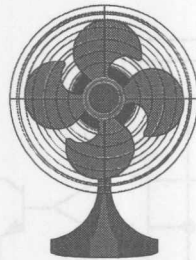
Airflow/Temperature Sensor “Cooling” Monitor/Controller



- Internal 100 ohm Heater Emulates Power IC
- Resistor-Programmable HI-LO Setpoints and Hysteresis
 - Internal 2.5V Reference
 - 5 mV/deg C Internal Scale Factor



TMP-12 Key Specs and Features (con't)

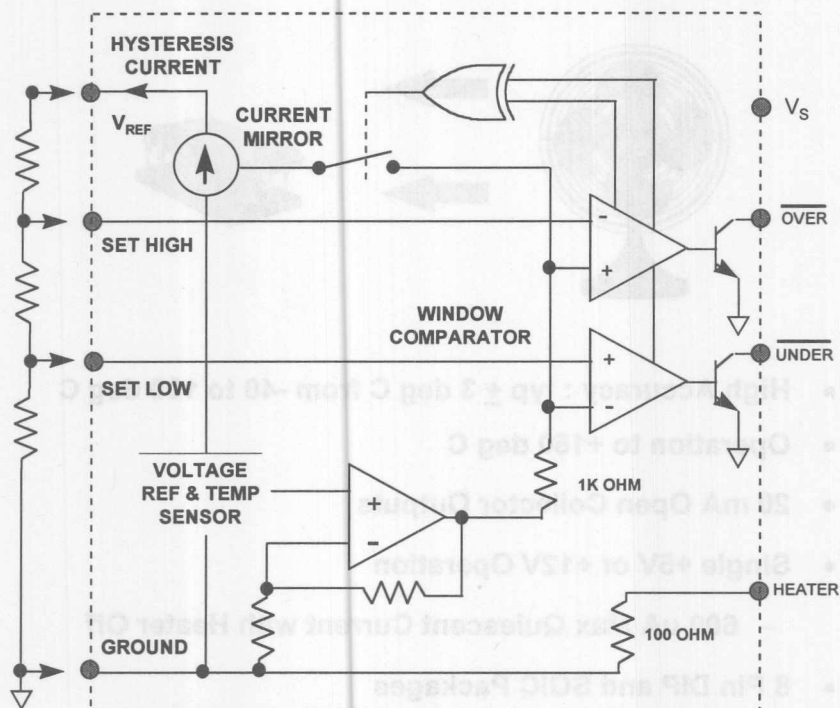


- High Accuracy : typ ± 3 deg C from -40 to 100 deg C
- Operation to +150 deg C
- 20 mA Open Collector Outputs
- Single +5V or +12V Operation
 - 600 μ A Max Quiescent Current with Heater Off
- 8 Pin DIP and SOIC Packages

11-33



TMP-12 Simplified Diagram



11 - 34



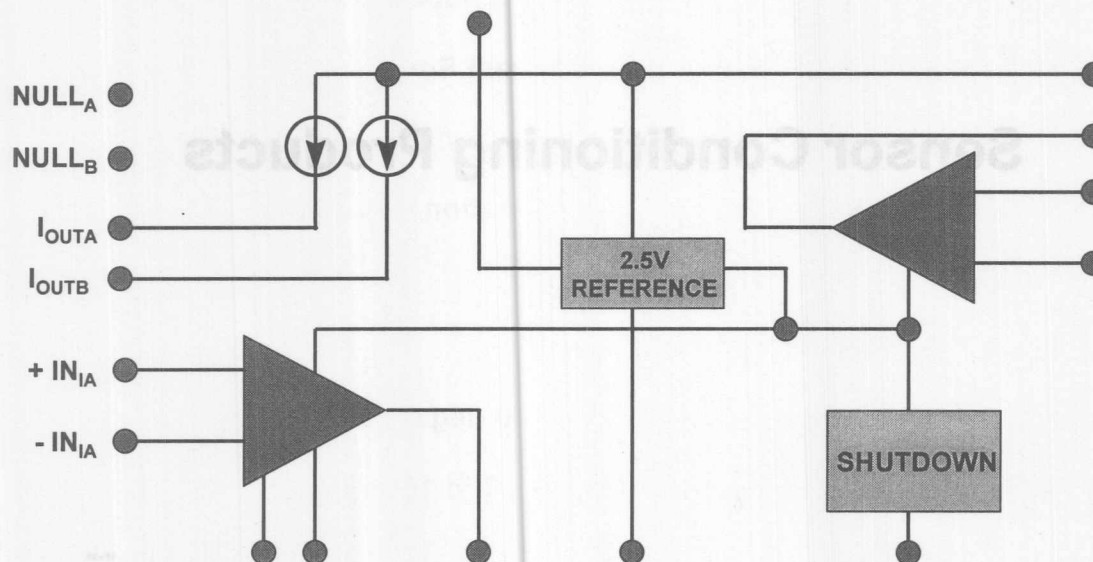
Sensor Conditioning Products

11 - 35



ADT70 Platinum RTD Conditioning Circuit

The ADT70 provides the complete signal conditioning solution for Platinum RTD temperature measurements!



11 - 36



ADT70- Key Specs and Features

- **Complete, PRTD Signal Conditioning Solution :**
 - **Matched 1mA (nominal) RTD Current Sources**
 - **Rail-Rail Output *Instrumentation Amplifier***
 - **Uncommitted Rail-Rail Output Operational Amplifier**
 - **On-Board 2.5V Reference**
- **Optimized for 1k ohm Platinum RTD**
- **Measures RTD Temperatures from -50 deg C to 500 deg C**
- **Extended Performance from -200 deg C to 1000 deg C**

11 - 37



ADT70- Key Specs and Features (con't)

- **High Accuracy :**
 - ± 0.1 deg C typ Error over RTD Range
 - ± 15 ppm/deg C Tempco
- **Single +5V or Dual ± 5 V Operation**
- **Low Current Consumption :**
 - 3 mA Normal
 - 10 uA Max in SHUTDOWN
- **-40 deg C to +125 deg C Operating Temp Range**
- **20 Pin DIP and SOIC Packages**



AD594, AD595 Monolithic Thermocouple Amplifiers

**A Complete Instrumentation Amplifier and Cold
Junction Compensation on a Single Chip!**

- Pretrimmed for Type J (AD594) or
- Type K (AD595) Thermocouples
- Can Be Used with Type T Thermocouple Inputs
- Low Impedance Voltage Output: 10 mV/deg C
- Built-In Ice Point Compensation
- Wide Power Supply Range: +5 V to ± 15 V
- Low Power: <1 mW typical
- Thermocouple Failure Alarm
- Laser Wafer Trimmed to 1 deg C Calibration Accuracy
- Setpoint Mode Operation
- Self-Contained Celsius Thermometer Operation
- High Impedance Differential Input
- Side-Brazed DIP or Low Cost Cerdip

11 - 39



AD596, AD597

Thermocouple Conditioner and Set Point Controller

The AD596 and AD597 are similar in design to the AD594 and AD595, but are optimized as set point controllers

- Operates with Type J (AD596) or Type K (AD597) Thermocouples
- Built-In Ice Point Compensation
- Temperature Proportional Operation – 10 mV/deg C
- Temperature Setpoint Operation – ON/OFF
- Programmable Switching Hysteresis
- High Impedance Differential Input Single (+5V to +30V) or Dual ($\pm 18V$) Power Supply Operation
- Supply Current only 160 μA
- 10 Pin TO-100 Metal Can or 8 Pin SOIC (AD597, only) Packages

11-40



Monolithic Accelerometers



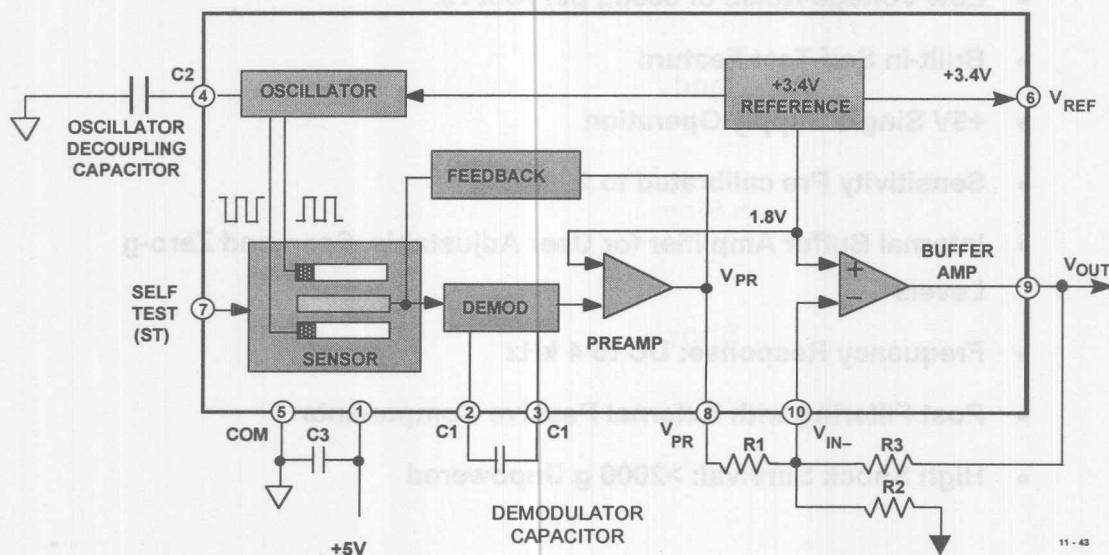
Where Are Accelerometers Used?

- **Measurement of Gravity to Determine Orientation:**
 - Tilt and Inclination
 - Position in 2 and 3 Dimensional Space
- **Inertial Measurement of Velocity and Position:**
 - Acceleration Single Integrated for Velocity
 - Acceleration Double Integrated for Position
- **Vibration and Shock Measurement:**
 - Measuring Vibration for Machine Health
 - Motion and Shock Detection



ADXL05 Monolithic $\pm 5g$ Accelerometer With Signal Conditioning

The ADXL05 is a complete acceleration measurement system in a single monolithic IC!



11 - 43



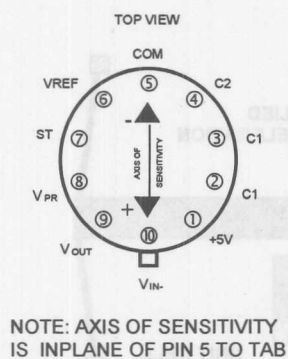
ADXL05 - Key Specs and Features

- Full-Scale Measurement Range: $\pm 5g$
- Low Voltage Noise of 500 μg per root Hz
- Built-in Self-Test Feature
- +5V Single Supply Operation
- Sensitivity Pre calibrated to 200mV/g
- Internal Buffer Amplifier for User Adjustable Span and Zero-g Levels
- Frequency Response: DC to 4 kHz
- Post Filtering with External Passive Components
- High Shock Survival: >2000 g Unpowered

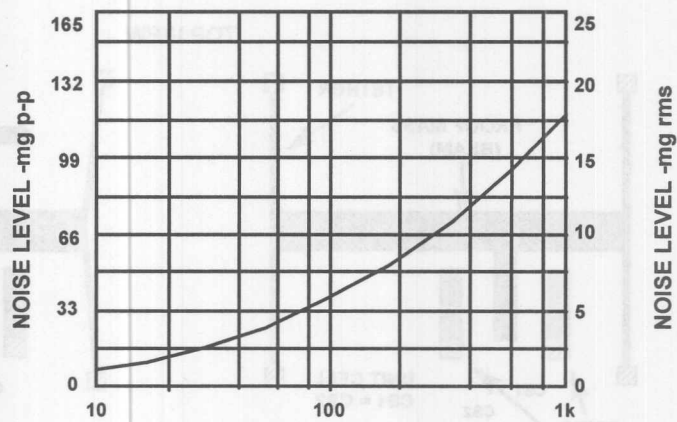
11 - 44



ADXL05 - Noise Level vs Bandwidth



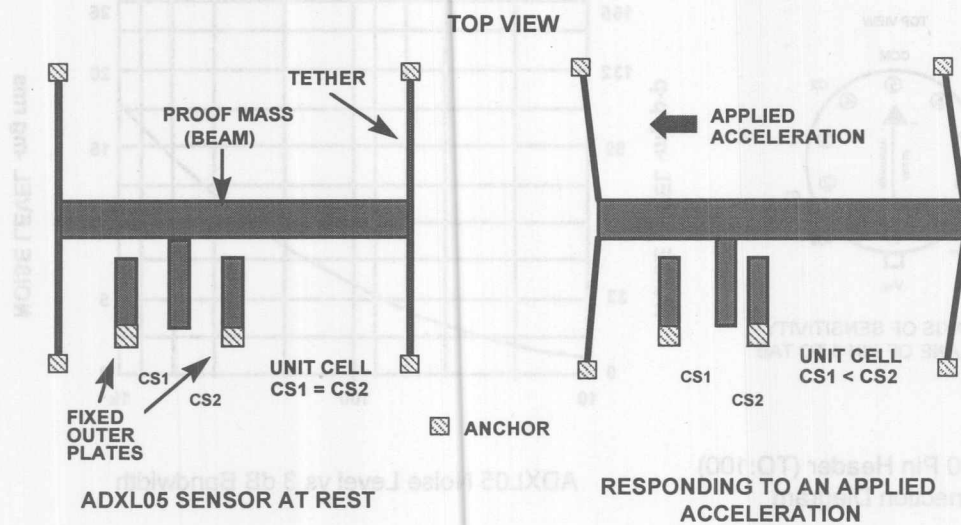
ADXL05 10 Pin Header (TO:100)
Connection Diagram



ADXL05 Noise Level vs 3 dB Bandwidth



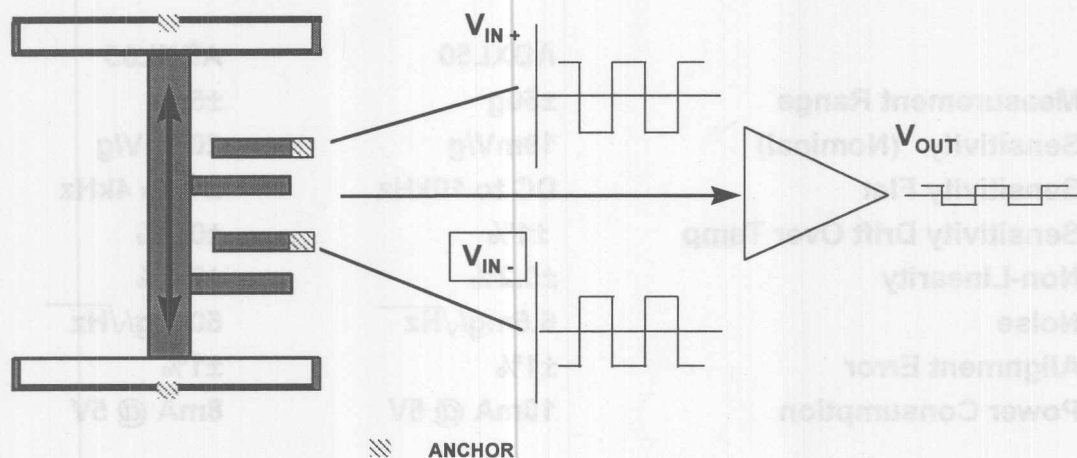
How Does the ADXL05 Work?



11 - 46



How Does the ADXL05 Work (con't)?



Drive Signals are 180 Degrees Out of Phase. When the Differential Capacitors are Unequal, There is a Signal Out of the Sensor which is Proportional to the Force on the Beam.

11 - 47



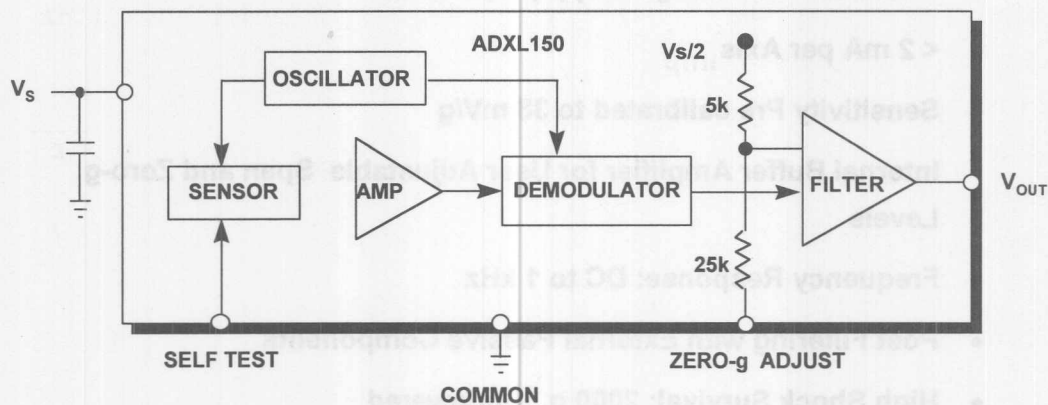
A Comparison of the ADXL05 to the ADXL50...

	ADXL50	ADXL05
• Measurement Range	±50g	±5g
• Sensitivity (Nominal)	19mV/g	200mV/g
• Sensitivity Flat	DC to 10kHz	DC to 4kHz
• Sensitivity Drift Over Temp	±1%	±0.5%
• Non-Linearity	±0.2%	±0.2%
• Noise	6.5mg/√Hz	500μg/√Hz
• Alignment Error	±1%	±1%
• Power Consumption	10mA @ 5V	8mA @ 5V



ADXL150 and ADXL250 $\pm 5g$ to $\pm 50g$ Single/Dual Axis Accelerometers

The ADXL150 and ADXL250 are monolithic, single and dual axis accelerometers. These improved replacements for the ADXL50 offer lower noise, wider dynamic range, reduced power consumption and improved zero g bias



11 - 49



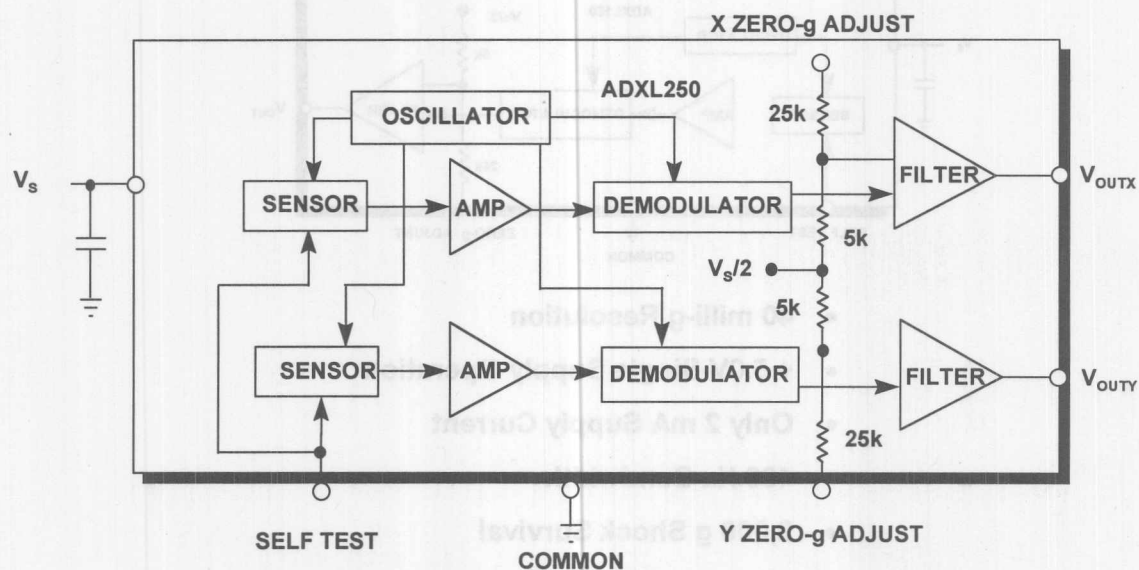
ADXL150, ADXL250 - Key Specs and Features

- **Pin Programmable Range of ± 50 g or ± 25 g**
- **Low Voltage Noise of 1 mg per root Hz**
- **Built-in Self-Test Feature**
- **+ 4.0V to + 6.0V Single Supply Operation**
- **< 2 mA per Axis**
- **Sensitivity Pre calibrated to 38 mV/g**
- **Internal Buffer Amplifier for User Adjustable Span and Zero-g Levels**
- **Frequency Response: DC to 1 kHz**
- **Post Filtering with External Passive Components**
- **High Shock Survival: 2000 g, Unpowered**

11 - 50



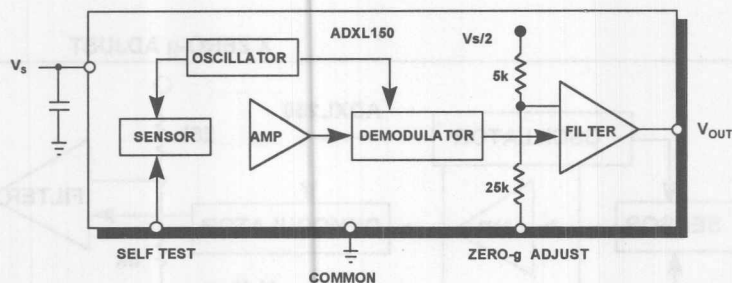
ADXL250 - Simplified Diagram



11-51



ADXL190 ± 100 g Single Axis Accelerometer



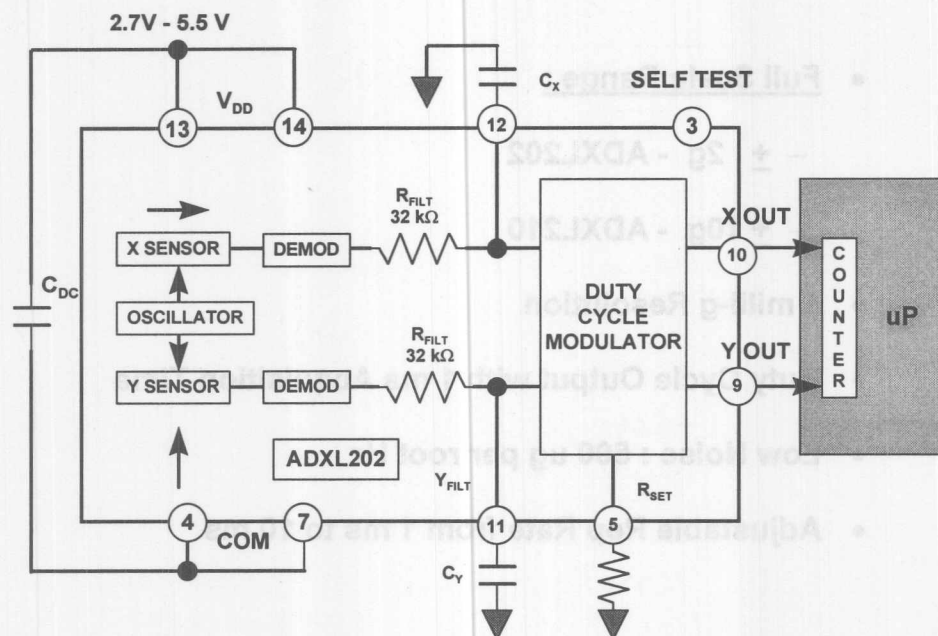
- 40 milli-g Resolution
- + 5.0V Single Supply Operation
- Only 2 mA Supply Current
- 400 Hz Bandwidth
- 2,000 g Shock Survival
- 14 Pin Surface Mount Cerpak

11 - 52



ADXL202, ADXL210

Low Cost, 2g/10g Dual Axis Accelerometers



11 - 53



ADXL202, ADXL210 - Key Specs and Features

- Full Scale Range :
 - $\pm 2g$ - ADXL202
 - $\pm 10g$ - ADXL210
- 5 milli-g Resolution
- Duty Cycle Output with 1 ms Acquisition Time
- Low Noise : 500 μg per root Hz
- Adjustable Rep Rate from 1 ms to 10 ms

11 - 54



**ADXL202, ADXL210 -
Key Specs and Features (con't)**

- **Bandwidth Adjustable via External Capacitors**
- **+ 2.7 V to + 5.5 V Operation**
- **Less than 600 uA Quiescent Current**
- **14 Pin Hermetic Surface Mount Cerpak**
- **0 deg C to 70 deg C Temperature Range**
- **1,000 g Shock Survival**

11 - 55



Key Specs and Features (cont)
ADXL202, ADXL210 -

- Bandwidth Adjustable via External Capacitors
- $+2.7\text{ V to }+5.5\text{ V}$ Operation
- Less than 800 μA Quiescent Current
- 14 Pin Hermetic Surface Mount Cerpak
- $0\text{ deg C to }70\text{ deg C}$ Temperature Range
- 1,000 g Shock Survival

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Section 12

Video Graphics Products

RGB to NTSC/PAL Analog Encoder

Digital Video Encoders

Digital Video Decoders

D/A Converters for Video Graphics



Section 12 Video Graphics Products

D/A Converters for Video Graphics
Digital Video Decoders
Digital Video Encoders
RGB to NTSC/PAL Analog Encoder



RGB to NTSC/PAL Analog Encoder



*** Preliminary**

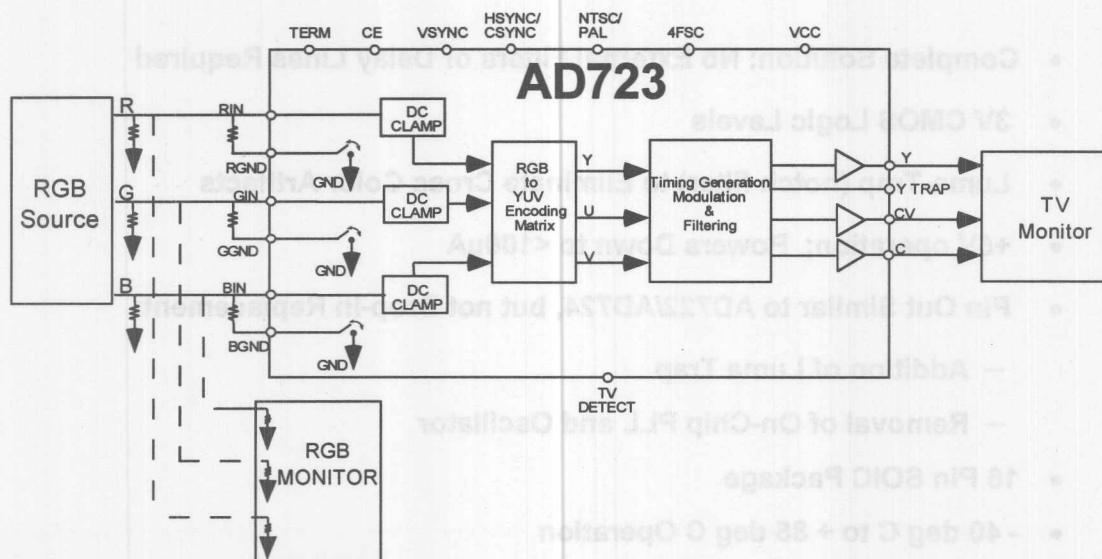
AD723*
Low Cost RGB to NTSC/PAL Encoder

- **Complete Solution: No External Filters or Delay Lines Required**
- **Luma-Trap (notch filter) to Eliminate Cross Color Artifacts**
- **+3V operation; Powers Down to <10uA**
- **Unique, Triple RGB Termination Switch for Load Maintenance**
- **Supports PC-98 "TV Presence Detect" Requirement**
- **Current Output Eliminates "large" 220 uF Capacitors**
- **24 Pin TSSOP Package**
- **- 40 deg C to + 85 deg C Operation**

12 - 4



AD723 Block Diagram





AD725

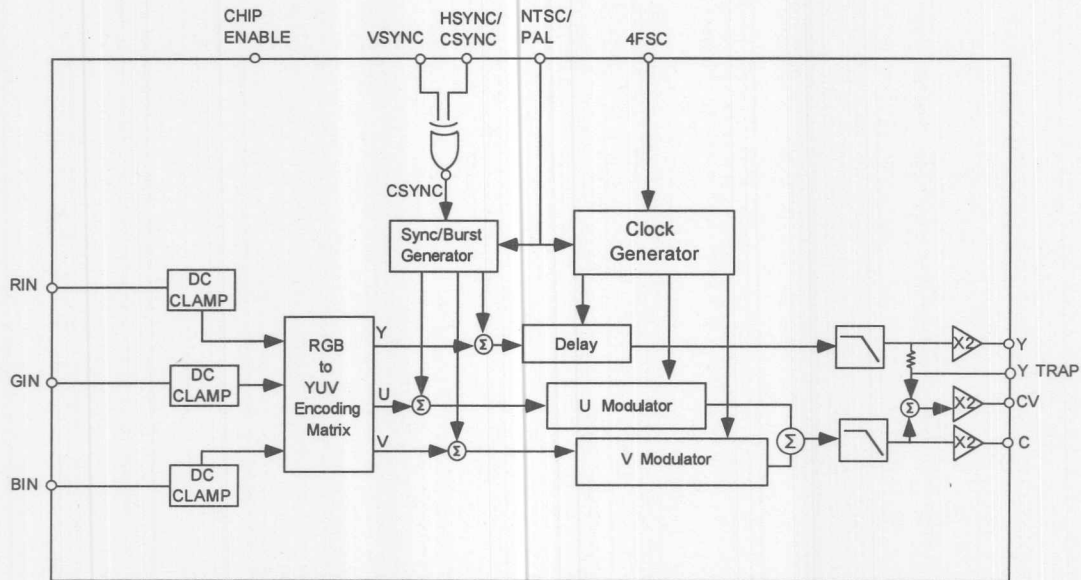
Very Low Cost RGB to NTSC/PAL Encoder

- **Complete Solution: No External Filters or Delay Lines Required**
- **3V CMOS Logic Levels**
- **Luma-Trap (notch filter) to Eliminate Cross Color Artifacts**
- **+5V operation; Powers Down to <100uA**
- **Pin Out Similar to AD722/AD724, but not Drop-In Replacement:**
 - **Addition of Luma Trap**
 - **Removal of On-Chip PLL and Oscillator**
- **16 Pin SOIC Package**
- **- 40 deg C to + 85 deg C Operation**

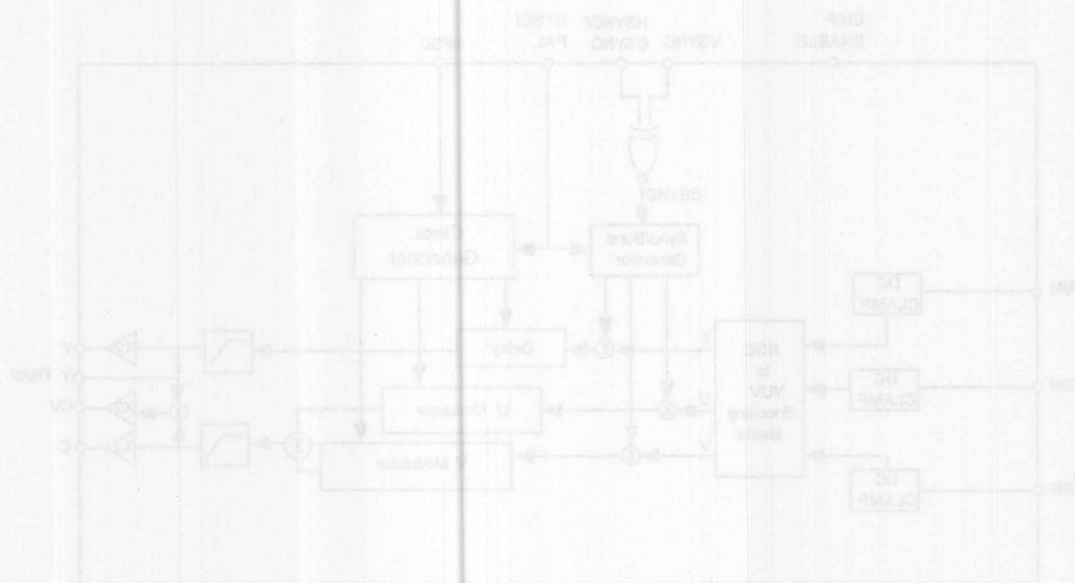
12 - 6



AD725 Block Diagram



12-7



12-8



Digital Video Encoders



What Are Digital Video Encoders?

A *Digital Video Encoder* converts Digital Component Video Data (CCIR-601 4:2:2) into a standard analog baseband television signal compatible with NTSC, PAL B/D/G/H/I, PAL M or PAL N. In addition to the Composite output signal, there is often the facility to output S-VHS Y/C, RGB or YUV Video.

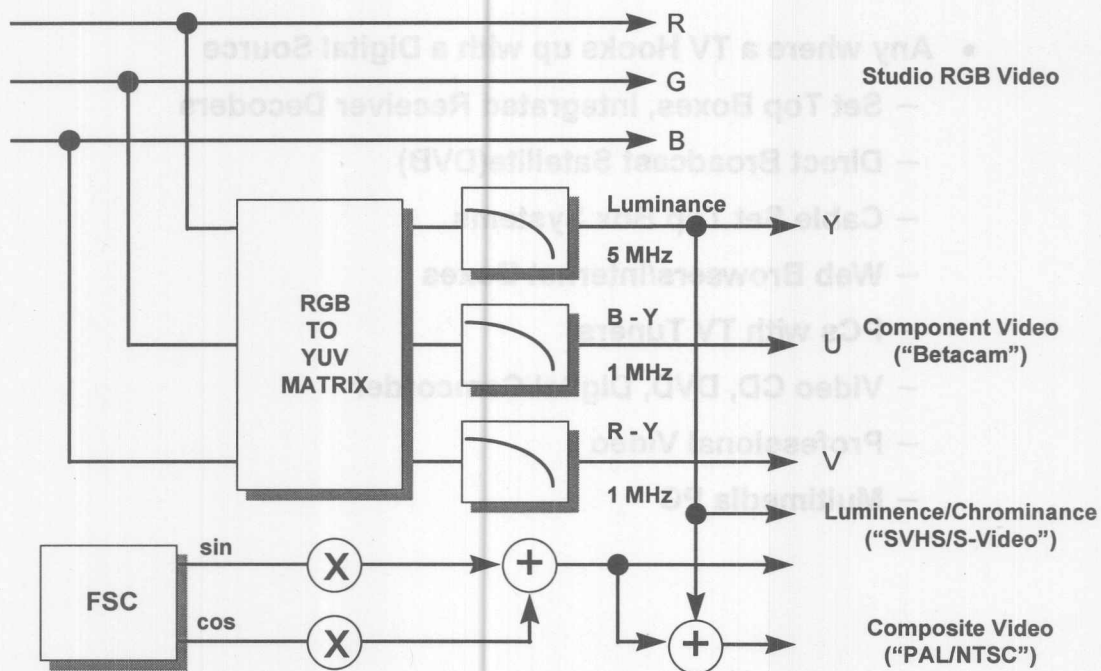


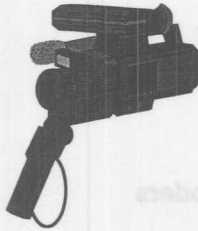
Where are (Digital) Video Encoders Used?

- **Any where a TV Hooks up with a Digital Source**
 - **Set Top Boxes, Integrated Receiver Decoders**
 - **Direct Broadcast Satellite(DVB)**
 - **Cable Set Top Box Systems**
 - **Web Browsers/Internet Boxes**
 - **PCs with TV Tuners**
 - **Video CD, DVD, Digital Camcorder**
 - **Professional Video**
 - **Multimedia PC**



Video Signal Formats...





Video Formats (con't)

- $\text{Luminance} = 0.299R + 0.578G + 0.114B$
- $U = 0.492 (B-Y)$
- $V = 0.877 (R-Y)$
- $\text{CHROMA} = U \sin(wt) + V \cos(wt) = A \sin(wt + O)$
- $A = \text{Saturation}, O = \text{Hue}$
- $3.58 \text{ MHz} = \text{NTSC}$
- $4.43 \text{ MHz} = \text{PAL}$



Digital Video Encoder Product Family

- **ADV7175A, ADV7176A**
- **ADV7177, ADV7178**
- **ADV7174**
- **ADV7170, ADV7171**
- **ADV7172, ADV7173**
- **10 Bit, High Quality Video Encoders with/without MACROVISION™**
- **9 Bit, Lower Cost Versions of ADV7175A and ADV7176A**
- **Similar to ADV7176A, No Teletext Insertion, Adds OSD (On Screen Display)**
- **Next Generation ADV7175A, ADV7176A, Adds CGMS-A and WSS (Wide Screen Signalling)**
- **Advanced 6 DAC NTSC/PAL Encoder with SSAFTM and Color Processing Control/MACROVISION™**

12 - 14



What is MacroVision?

- **“Pay-per-View” Copy Protection System**
- **Prevents Users from Making Unauthorized Copies of Digitally-Transmitted Pay Per View Videos using a VCR (Rev 6.0)**
- **Rev 7.1 Set for NTSC/PAL**
- **License Required to Purchase ADV7175A**



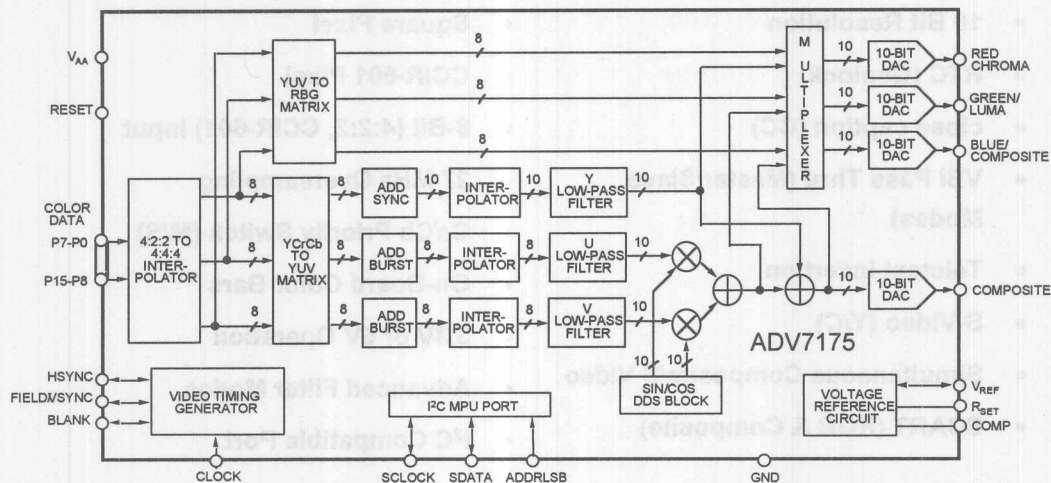
ADV7175A and ADV7176A

- **The ADV7175A Has the Additional Feature of the Macrovision (Revision 7.1) Anticopy Algorithm.**
- **ADV7176A Fully Backward Compatible (software, hardware and pinout) with ADV7176**
- **ADV7175A Hardware and Pinout Compatible, but Requires Programming Edits for Rev 6.1 or Rev 7.01**

12 - 16



ADV7175A and ADV7176A - Simplified Diagram



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ADV7175A, ADV7176A - Key Specs and Features

- 4 D/A Converters
- 10 Bit Resolution
- RTC (Genlock)
- close caption (CC)
- VBI Pass Thru (Master/Slave Modes)
- Teletext Insertion
- S-Video (Y/C)
- Simultaneous Composite/S Video
- SCART (RGB & Composite)
- YUV Output
- Square Pixel
- CCIR-601 Pixel
- 8-Bit (4:2:2, CCIR-601) Input
- 27 MHz Oversampling
- Cr/Cb Priority Switch (M/S)
- On-Board Color Bars
- 3.3V or 5V Operation
- Advanced Filter Modes
- I²C Compatible Port

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ADV7177 and ADV7178

The ADV7177 and ADV7178 are lower cost versions of the ADV7175A and ADV7176A, respectively

Includes...

- 3 D/A Converters
- 9 Bit Resolution
- On Screen Display (OSD) - ADV7177, Only
- 13.5 MHz Clock Out Support
- Crystal Output

Does Not Include...

- RTC Genlock Feature
- Teletext Insertion
- SCART (RGB & Composite)
- YUV Output

12 - 19



ADV7174

- **Similar to ADV7176A**

Includes...

- **On-Screen Display (OSD)**

Does Not Include...

- **Teletext Insertion**



ADV7172/ADV7173 Advanced NTSC/PAL Digital Video Encoder

The ADV7172 and ADV7173 feature SSAF™ (Super Sub-Aliasing Filter) and Color Processing Control/Macrovision

- Support for PAL B/D/G/H/I, PAL M, PAL N, PAL-60 & NTSC
- Macrovision 7.01 support
- External PAL/NTSC selection pin
- 6 DAC's Outputs, simultaneous CVBS, Y/C & YUV/RGB (Betacam, SMPTE & MII)
- Contrast, Brightness, Hue & Saturation controls
- Additional timing signals (HSO, VSO, CSO & Clamp)
- WSS, CGMS, Closed Captioning, Teletext & other VBI data insertion

12-21



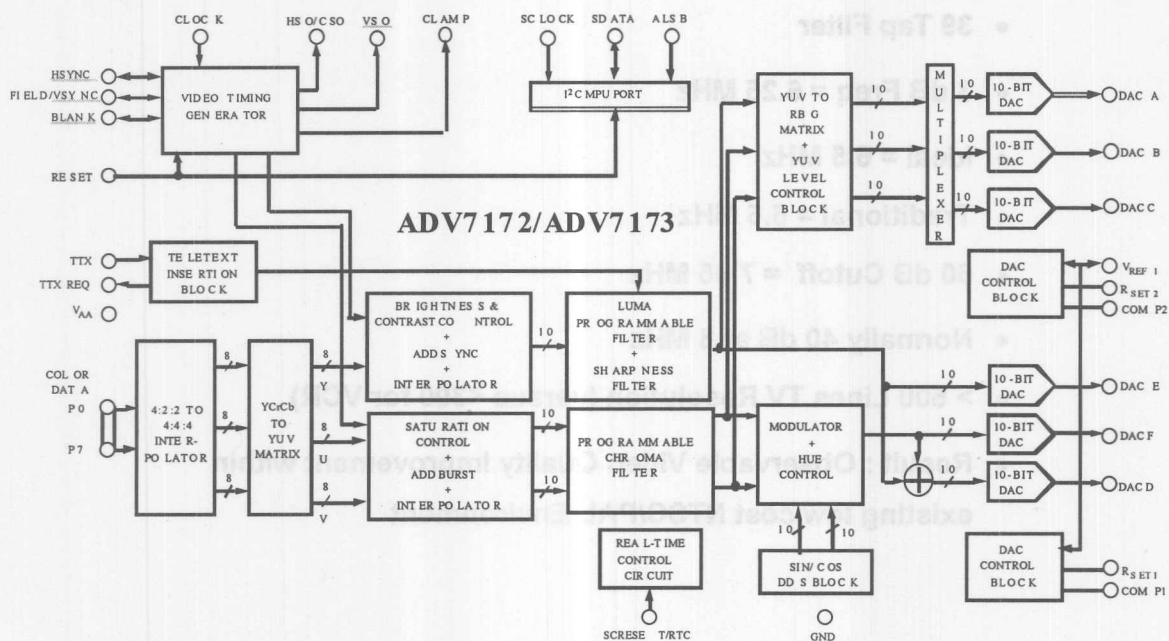
ADV7172, ADV7173 - Key Specs and Features (con't)

- **Advanced Power Management features:**
 - 5V/3V Operation
 - Individual DAC ON/OFF Control
 - DAC Low Power Mode
 - Ultra low Sleep current (200nA)
 - Intelligent TV detection feature
 - Support for DAC buffering
- **Advanced Power-on Reset**
- **Fast I²C Control**

12 - 22



ADV7172, ADV7173 - Block Diagram



12-23



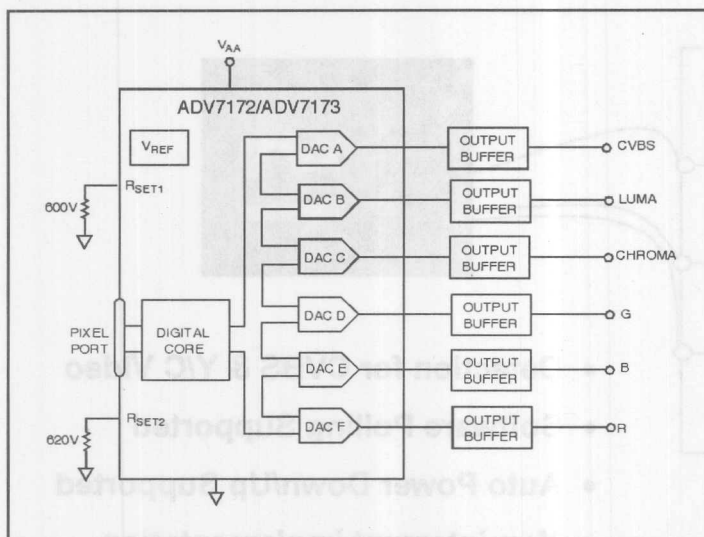
Increased DVD Display Resolution with SSAF™

- 39 Tap Filter
- 3 dB Freq = 6.25 MHz
- Ideal = 6.5 MHz
- Traditional = 5.5 MHz
- 60 dB Cutoff = 7.95 MHz
- Normally 40 dB at 8 MHz
- > 500 Lines TV Resolution (versus <300 for VCR)
- Result : Observable Video Quality Improvement within existing low cost NTSC/PAL Environment

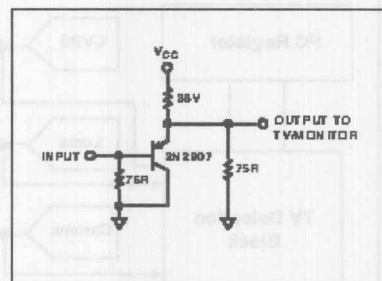
12-24



DAC Output Connection



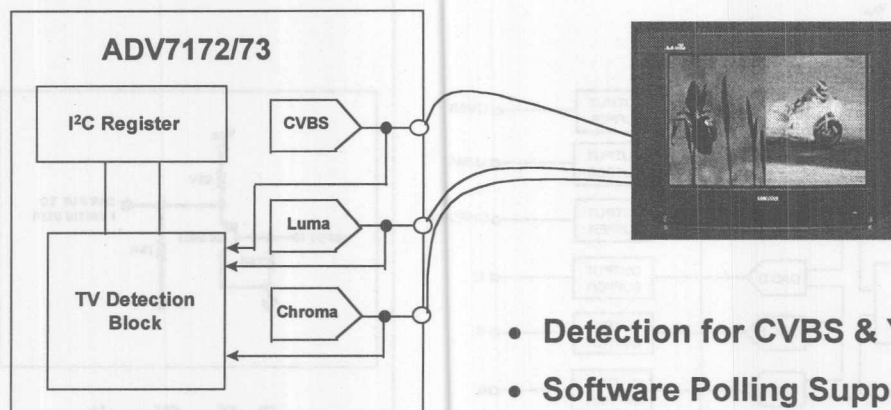
Output Configuration of DACs



Buffer Circuit



TV Auto-Detect



- **Detection for CVBS & Y/C Video**
- **Software Polling Supported**
- **Auto Power Down/Up Supported**
- **Non-interrupt implementation**

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Digital Video Decoders



What Are Digital Video Decoders?

A Digital Video Decoder converts CVBS, S-Video and YUV analog baseband television signals into Digital CCIR-601 4:2:2 Component Video compatible with NTSC, PAL B/D/G/H/I, PAL M or PAL N.



ADV7185

Video Decoder with Comb Filtering and H,V Scaling

The ADV7185 is an integrated Video Decoder that recognises analog baseband NTSC or PAL television signals and converts to Digital 4::2:2 or 4:1:1 Component Video Data in 16-bit CCIR601, 8-bit CCIR656 or extended 10-bit CCIR656 format.

There is the facility to input 6 Composite or 3 S-VHS Y/C Video signals or a combination of the two.

The ADV7185 modes are set up over a serial bi-directional 2 wire interface (I²C Compatible).



ADV7185 - Key Specs and Features

- **10-Bit A/D Converters with 57dB SNR**
- **Single 27 MHz Clock Required**
- **Real Time Horizontal and Vertical Scaling**
- **Luma and Chroma Comb Filtering**
- **Automatic NTSC/PAL Identification**
- **0.5V to 2.0V pk-pk Input Range**
- **Differential Gain < 1%**
- **Differential Phase < 1 Degree**
- **Programmable or Automatic Gain Control**
- **Programmable Peak White, Hue, Brightness, Saturation and Contrast**

12 - 30



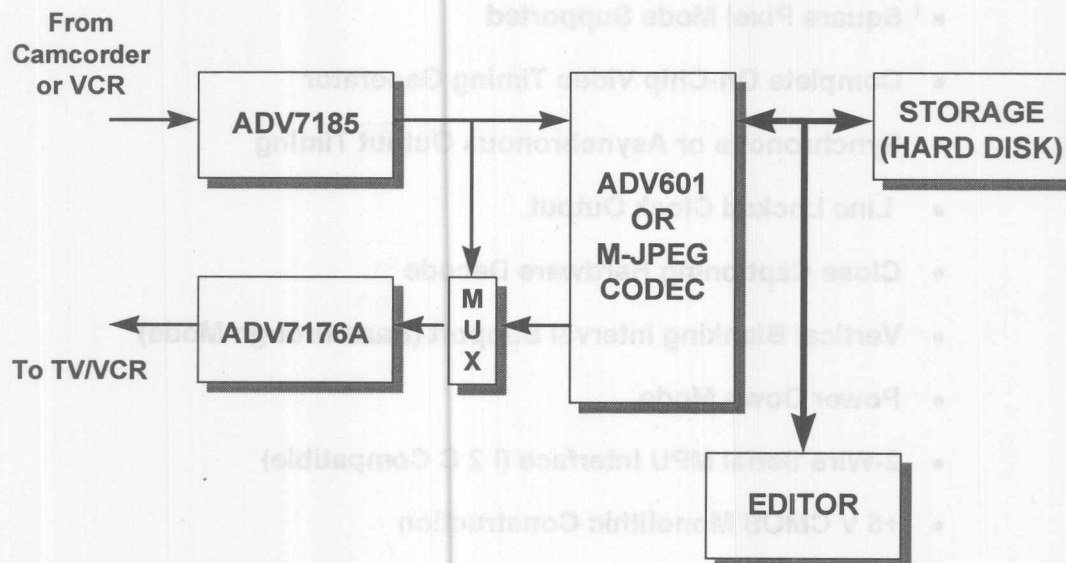
ADV7185 - Key Specs and Features (con't)

- **Square Pixel Mode Supported**
- **Complete On-Chip Video Timing Generator**
- **Synchronous or Asynchronous Output Timing**
- **Line Locked Clock Output**
- **Close Captioning Hardware Decode**
- **Vertical Blanking Interval Support (Passthrough Mode)**
- **Power Down Mode**
- **2-Wire Serial MPU Interface (I²C Compatible)**
- **+5 V CMOS Monolithic Construction**
- **80-Pin TQFP Thermally Enhanced Package**

12 - 31



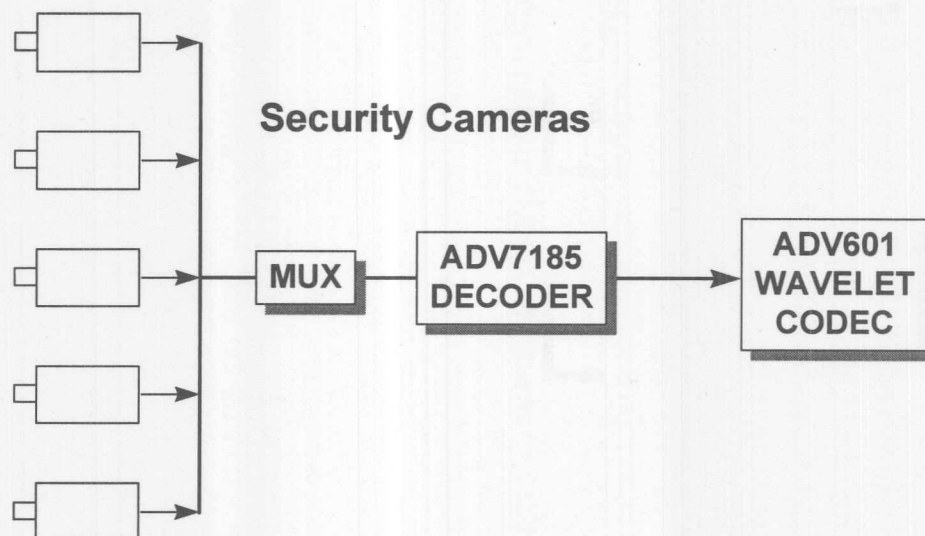
ADV7185 - Video Editing



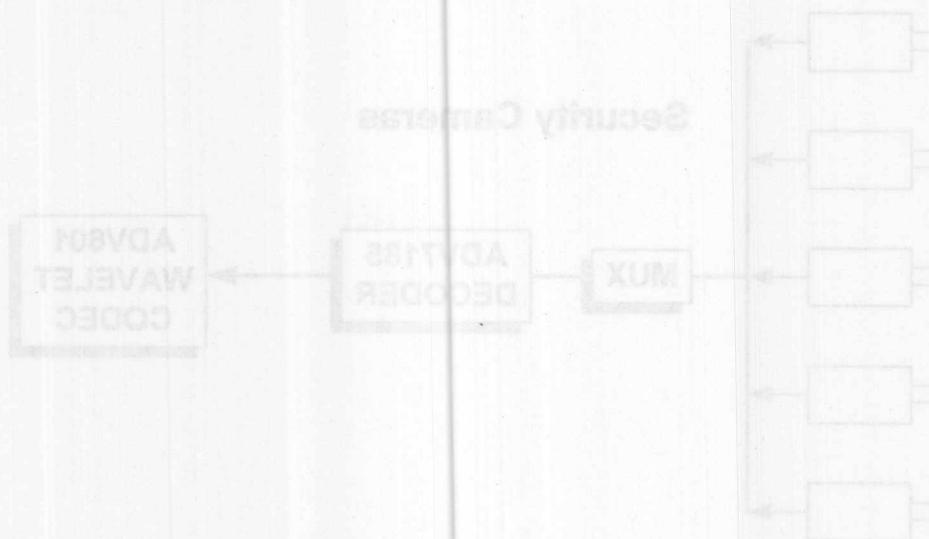
12 - 32



ADV7185 - Security Systems



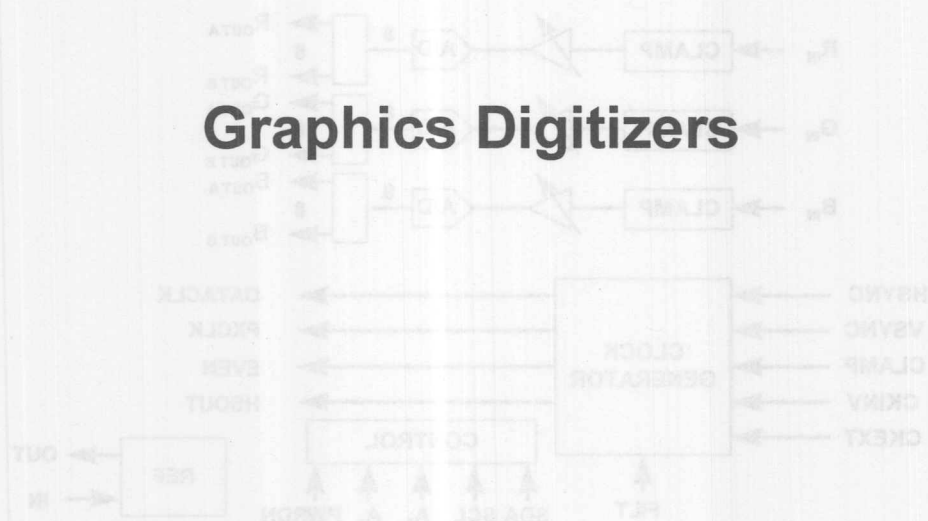
12 - 33



12 - 34



Graphics Digitizers

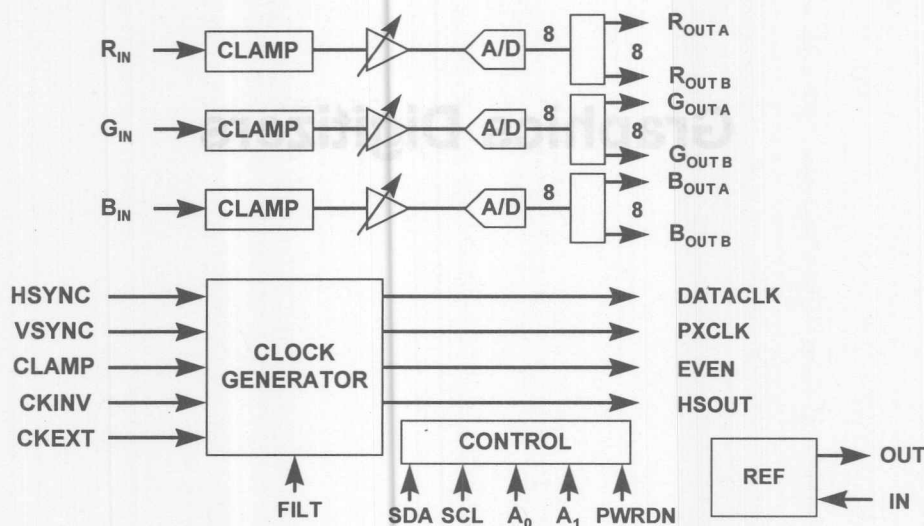




* Preliminary

AD9884* 8 Bit, 140 MSPS Graphics Digitizer

The AD9884 is a complete monolithic graphics digitizer optimized for digitizing RGB graphics signals from personal computers and workstations



12 - 36



AD9884 - Key Specs and Features

- **300 MHz Full Power Bandwidth Supports 1280 x 1024 Resolution @ 75 Hz**
- **On-Board PLL Generates Pixel Clock from 20-140 MHz**
- **PLL Clock Jitter Typically Only 500 ps peak-peak**
- **0.5 - 1.0 Volt Input Range**
- **Internal 1.25V Reference**
- **Programmable Gain and CLAMP Control**
- **Low Power : 3.3V @ 800 mW, typ**
- **128 Lead MQFP Package**
- **0 deg C to + 85 deg C Operation**

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AD9884 - Key Specs and Features

- 300 MHz Full Power Bandwidth Supports 1280 x 1024 Resolution @ 75 Hz
- On-Board PLL Generates Pixel Clock from 30-140 MHz
- PLL Clock Jitter Typically Only 800 ps peak-peak
- 0.5 - 1.0 Volt Input Range
- Internal 1.25V Reference
- Programmable Gain and CLAMP Control
- Low Power - 3.3V @ 500 mW typ
- 128 Lead MOPF Packages
- 0 deg C to + 85 deg C Operation

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D/A Converters for Video Graphics



ADV7123 and ADV7127 10-Bit, Single/Triple Video D/A Converters

The ADV7123 and ADV7127 are 10 Bit D/A Converters capable of generating RGB video output signals compatible with RS-343A and RS-170 broadcast standards.

- 140 MSPS Throughput Rates
- -48dB Spurious-Free Dynamic Range
- RS-343A/RS-170 Compatible Output
- TTL Compatible Inputs
- Internal Reference : $\pm 2\%$
- +5 V CMOS Monolithic Construction
- Low Power Dissipation
- Low Power Standby Mode
- 48-Pin TQFP Package
- Industrial Temperature Range : -40 deg C to +85 deg C

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Section 13

Embedded DSP-Based Motor Controllers



Why DSP In Motor Control?

- **Increased Performance With Higher Processing Power**
- **Real-Time Processing**
- **Flexibility**
- **Trend to Digital Control**
- **Integrated (Single Chip) Solution**



Why DSP In Motor Control?(con't)

- **Complex Mathematical Algorithms**
 - **Variable Speed Control**
 - **Vector Calculations - Park/Clark**
 - **Sensorless Control**
 - **Filtering**
 - **Noise & Vibration Reduction**
 - **Power Factor Correction**
 -

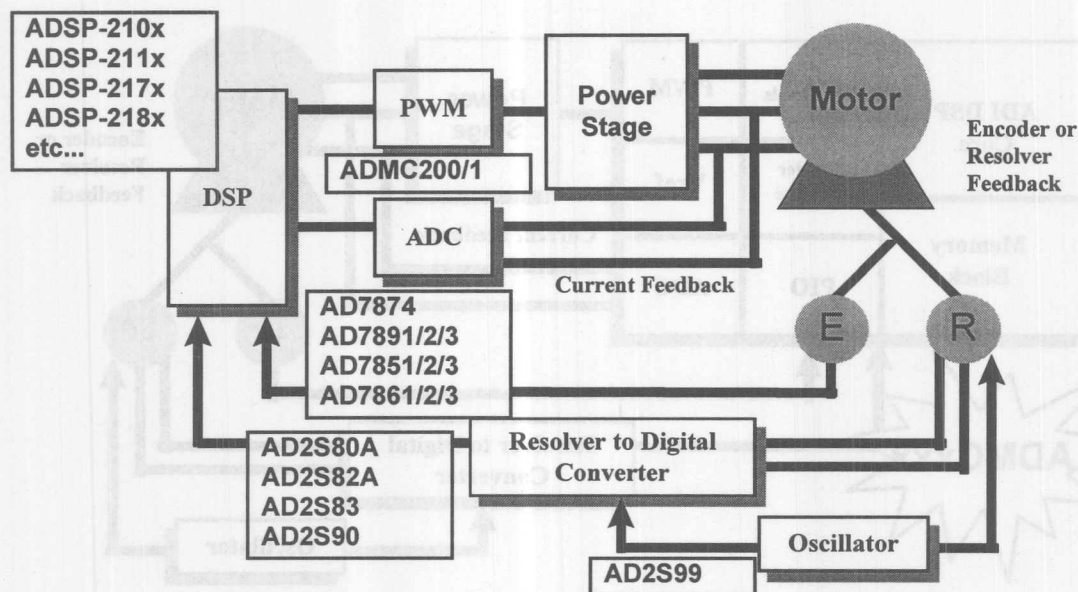


Applications for DSP Based Motor Control

- **Appliance**
 - Refrigeration Compressors
 - Washing Machine Motors
 - HVAC
 - Fans
 - Pumps
- **Industrial**
 - GP Motor Drives
 - Open Loop Inverters
 - Closed Loop Inverters
 - Servo Drives
- **Automotive**
 - Electric Vehicles
 - Power Steering
 - Active Suspension
 - HVAC
- **Other**
 - Uninterruptible Power Supplies
 - Electric Wheelchair
 - Electric Bicycle

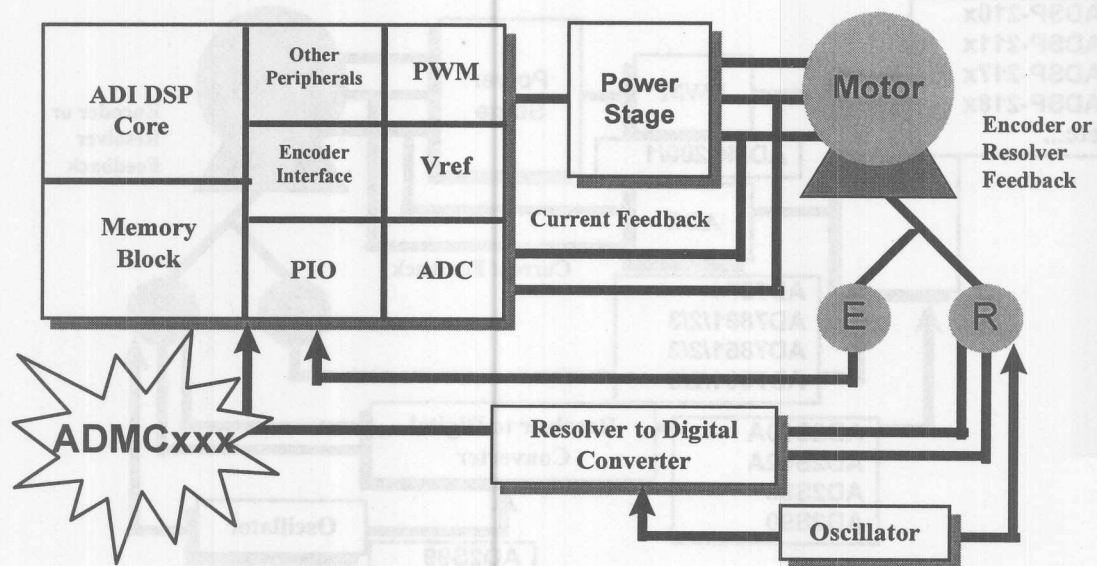


Analog & Digital IC Motor Control Signal Chain





ADI's System on a Chip...The Integrated Solution!

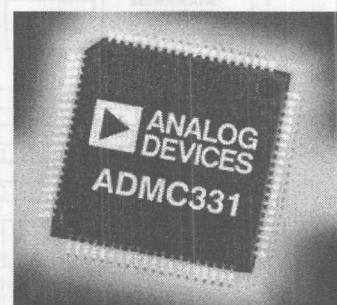




Analog Devices ADMC331

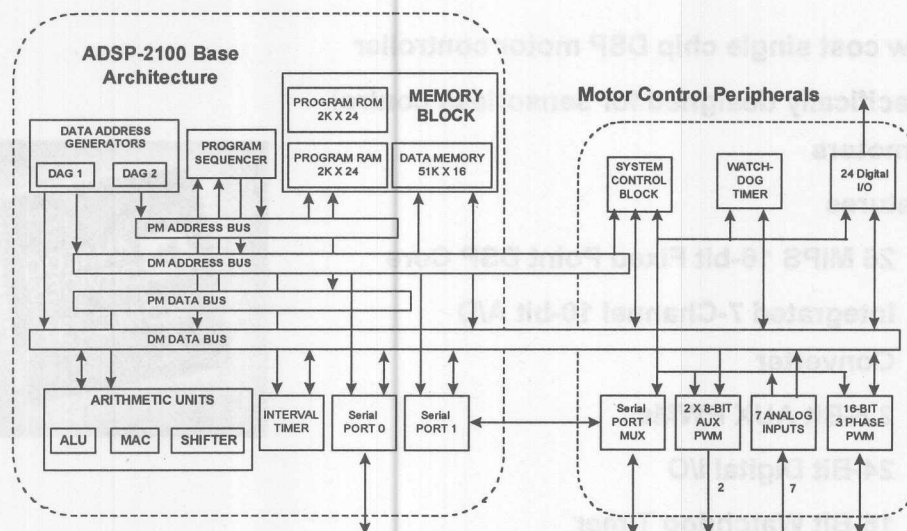
- **Low cost single chip DSP motor controller**
- **Specifically designed for sensorless control of motors**
- **Features**

- **26 MIPS 16-bit Fixed Point DSP Core**
- **Integrated 7-Channel 10-bit A/D Converter**
- **2 8-Bit AUX PWMs**
- **24-Bit Digital I/O**
- **16-Bit Watchdog Timer**
- **Two Synchronous Serial Ports**
-





ADMC331 Product Architecture





Analog Devices ADMC300

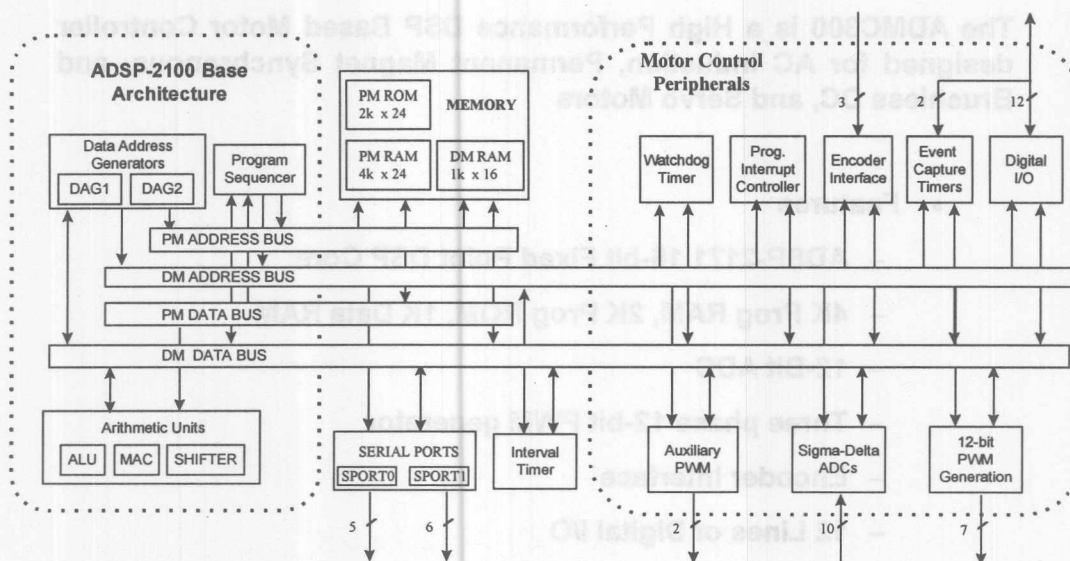
The ADMC300 is a High Performance DSP Based Motor Controller designed for AC Induction, Permanent Magnet Synchronous, and Brushless DC, and Servo Motors

- **Features**

- ADSP-2171 16-bit Fixed Point DSP Core
- 4K Prog RAM, 2K Prog ROM, 1K Data RAM
- 12-Bit ADC
- Three phase 12-bit PWM generator
- Encoder Interface
- 12 Lines of Digital I/O
- 2 Synchronous Serial Ports



ADMC300 Functional Block Diagram





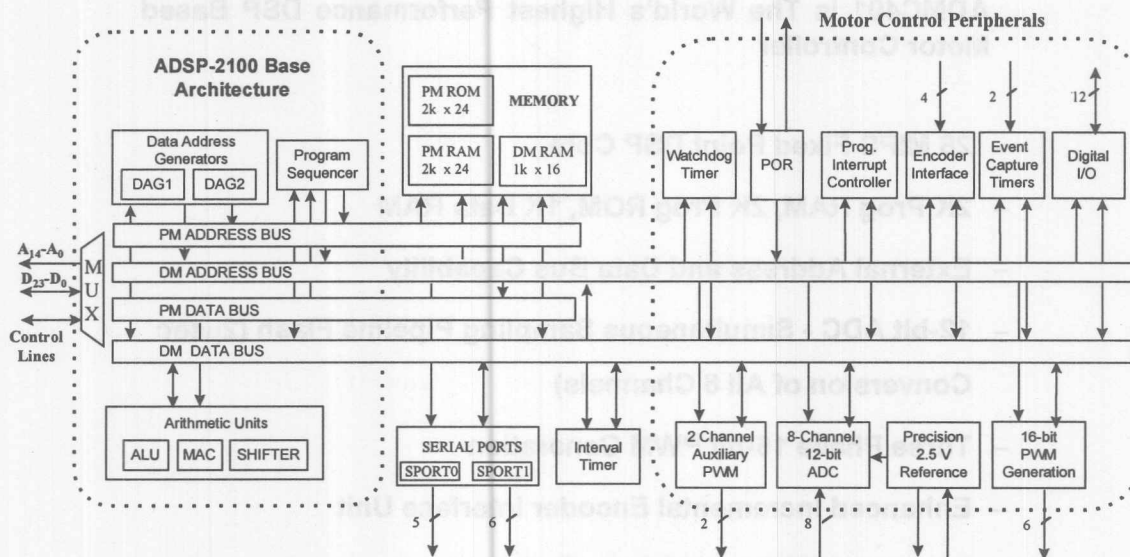
ADMC401 **Embedded DSP-based Motor Controller**

ADMC401 is The World's Highest Performance DSP Based Motor Controller

- **26 MIPS Fixed Point DSP Core**
- **2K Prog RAM, 2K Prog ROM, 1K Data RAM**
- **External Address and Data Bus Capability**
- **12-bit ADC - Simultaneous Sampling Pipeline Flash (2 μ sec Conversion of All 8 Channels)**
- **Three Phase 16-bit PWM Generation**
- **Enhanced Incremental Encoder Interface Unit**
- **Integrated POR and Voltage Reference**



ADMC401 High Performance DSP Motor Controller - Block Diagram



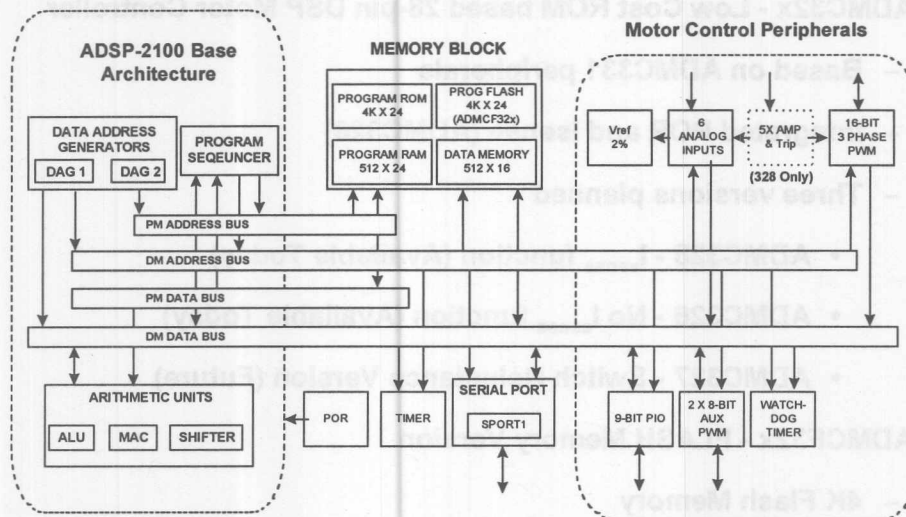


ADMCF32x and ADMC32x Product Families

- **ADMC32x - Low Cost ROM based 28-pin DSP Motor Controller**
 - Based on ADMC331 peripherals
 - Integrated POR and Isense (ADMC328)
 - Three versions planned
 - **ADMC328 - I_{sense} function (Available Today)**
 - **ADMC326 - No I_{sense} function (Available Today)**
 - **ADMC327 - Switch Reluctance Version (Future)**
- **ADMCF32x - FLASH Memory Version**
 - 4K Flash Memory
 - Pin for Pin Compatible with ADMC32x
 -



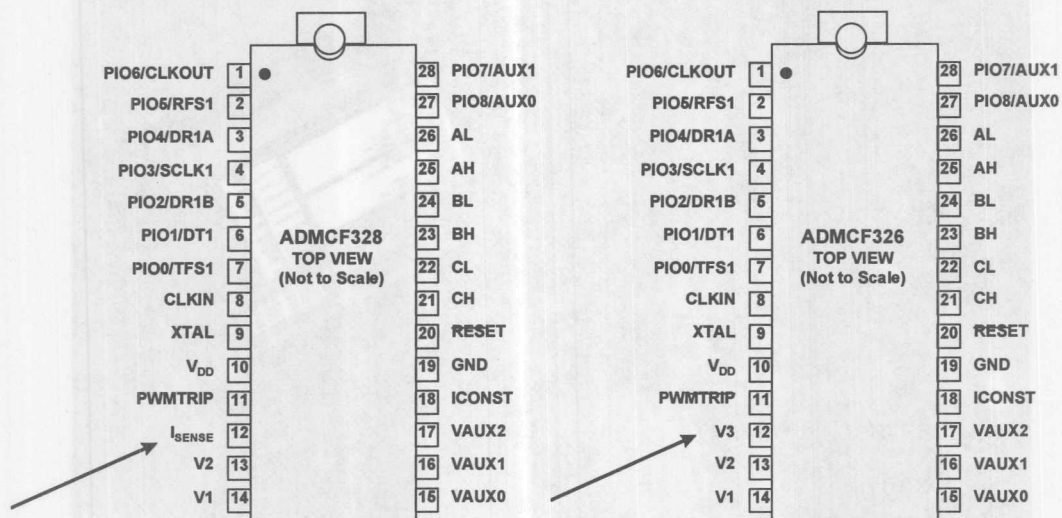
ADMCF32x / ADMC32x Product Architecture





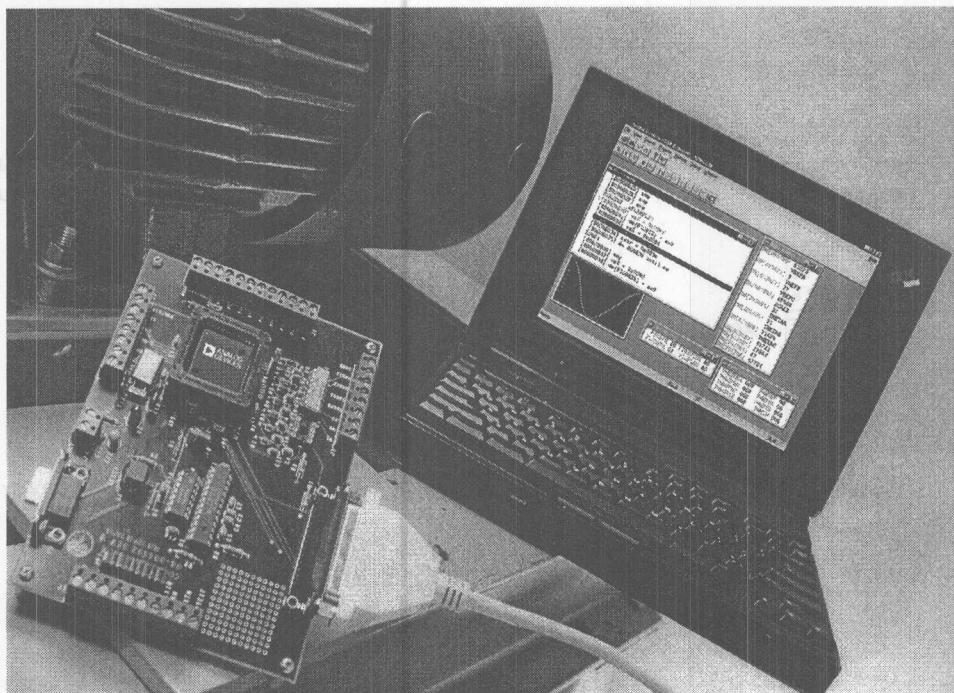
ADMCF32x and ADMC32x Pin Configuration

Low Cost Pin for Pin Compatible ROM and Flash Versions





ADI Development Tools



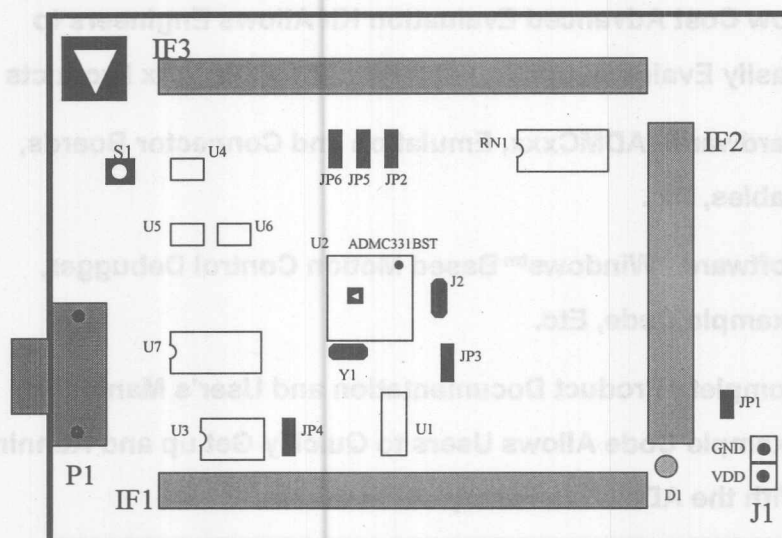


ADI Development Tools

- **Low Cost Advanced Evaluation Kit Allows Engineers to Easily Evaluate and Develop With the ADMCxxx Products**
- **Hardware - ADMCxxx, Emulation and Connector Boards, Cables, Etc.**
- **Software - Windows[™] Based Motion Control Debugger, Example Code, Etc.**
- **Complete Product Documentation and User's Manuals, Example Code Allows Users to Quickly Get up and Running With the ADMCxxx Family of Products**



ADMC331 Evaluation Board





Section 14

Analog Front End Processors

Voice Band CODECs

DSP Converters



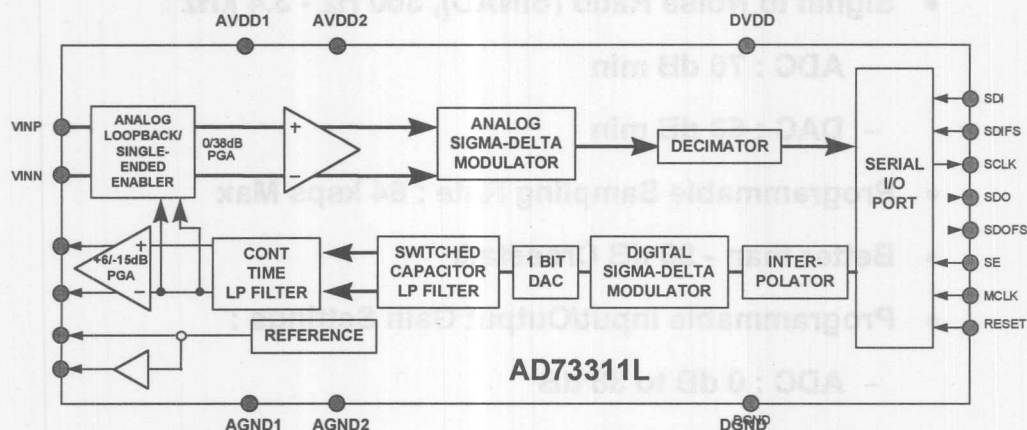
Section 14
Analog Front End Processors
Voice Band CODECs
DSP Converters



Preliminary
Information

AD73311L* Single Channel Voiceband CODEC

The AD73311L is a complete analog front-end processor for general purpose applications including speech and telephony. It is an enhanced version of our AD73311.





AD73311L - Key Specs and Features

- 16 Bit A/D and D/A Converters
- Programmable Input/Output Sample Rates
- Signal to Noise Ratio (SINAD), 300 Hz - 3.4 kHz :
 - ADC : 70 dB min
 - DAC : 63 dB min
- Programmable Sampling Rate : 64 ksps Max
- Better than - 90 dB Crosstalk
- Programmable Input/Output Gain Settings :
 - ADC : 0 dB to 38 dB
 - DAC : - 15 dB to + 6dB



AD73311L - Key Specs and Features

- **Flexible Serial Port Allows up to 8 Devices to be Connected in Cascade**
- **Single + 3V Operation**
- **50 mW Max Power Consumption @ + 2.7V**
- **On-Chip Reference**
- **20 Lead SOIC, SSOP and TSSOP Packages**
- **Evaluation Board Available :**
 - **EVAL-AD73311EB**
 - **EVAL-AD73311EZ (EZ Kit Lite)**



Programmable Sampling Rates

Master Clock (MCLK) :

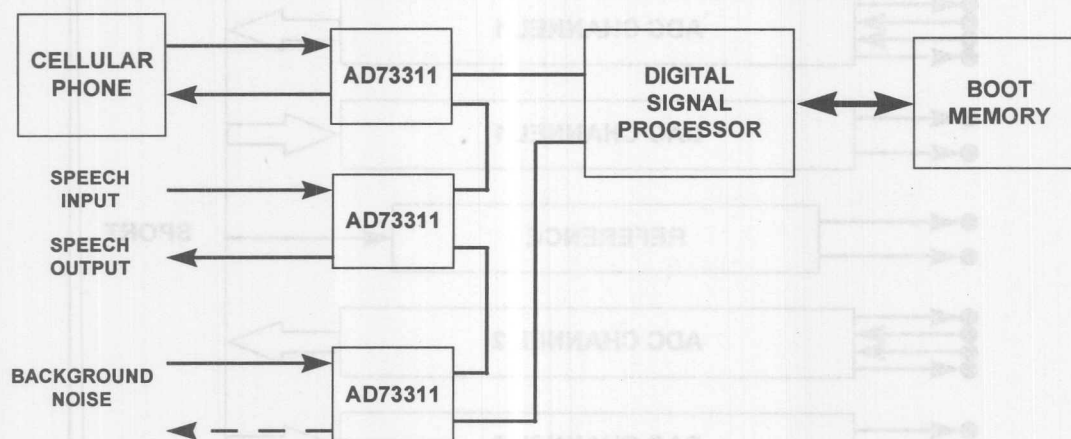
- ADC/DAC Sampling Rate is $MCLK/256$
- For $MCLK = 16.384$ MHz, Sampling Rate = 64 kHz (default)
- $MCLK \div N$; $N = 1, 2, 3, 4, 5$
- Sample Rates = 64 kHz, 32 kHz, 21.33 kHz, 16 kHz, 12.8 kHz

SPORT Serial Clock (SCLK) :

- $MCLK \div N$; $N = 2, 4, 8$
- Flexibility for Different Host DSP Clock Speeds



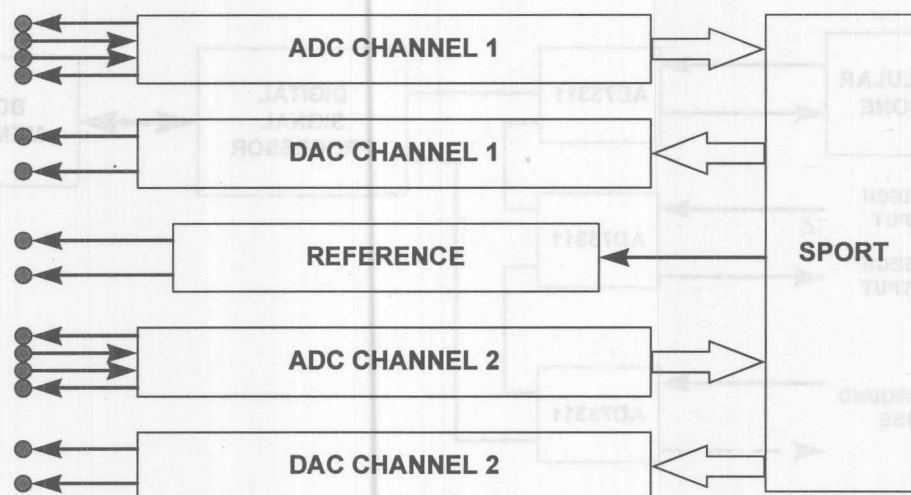
AD73311L Application : Hands-Free Accessories





AD73322 Dual Channel Voiceband CODEC

The AD73322 is essentially a dual channel version of the AD73311





AD73322 - Key Specs and Features

- **16 Bit A/D and D/A Converters**
- **Programmable Input/Output Sample Rates**
- **Signal to Noise Ratio (SINAD), 0 Hz - 4.0 kHz :**
 - **ADC : 70 dB min**
 - **DAC : 63 dB min**
- **64 Kilosamples/second Maximum Sampling Rate**
- **Better than - 90 dB Crosstalk**
- **Programmable Input/Output Gain Settings :**
 - **ADC : 0 dB to 38 dB**
 - **DAC : - 15 dB to + 6dB**



AD73322 - Key Specs and Features

- **Flexible Serial Port Allows up to 4 Dual Devices to be Connected in Cascade**
- **Single + 2.7V to + 5.5V Operation**
- **80 mW Max Power Consumption @ + 2.7V**
- **On-Chip Reference**
- **28 Lead SOIC and 44 Pin LQFP Packages**
- **Evaluation Board Available :**
 - **EVAL-AD73322EB**
 - **EVAL-AD73322EZ (EZ Kit Lite)**



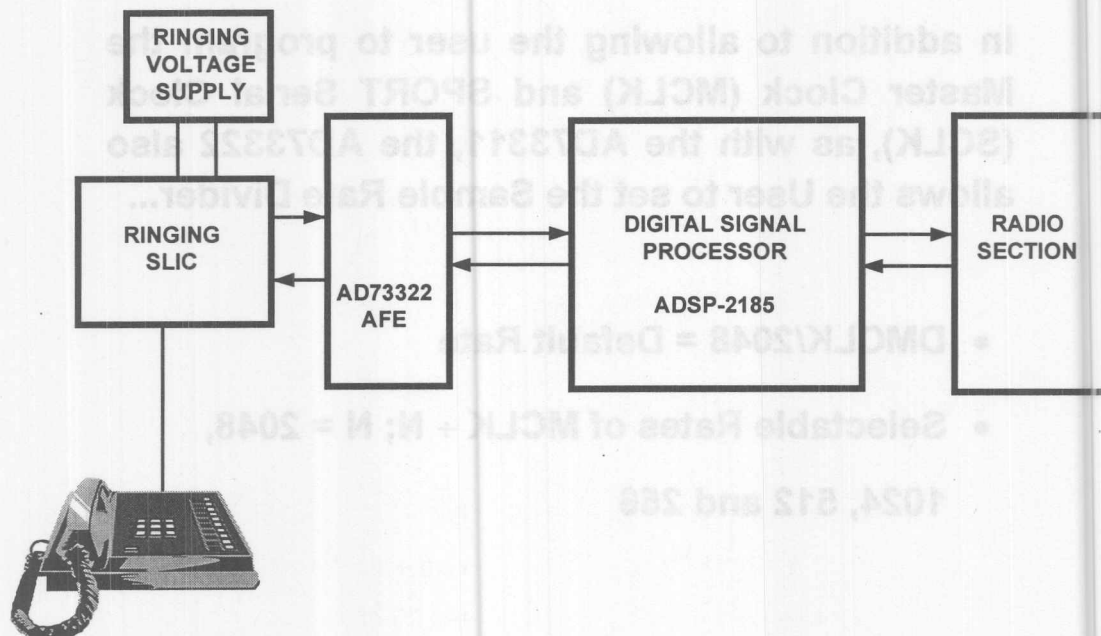
Programmable Sampling Rates

In addition to allowing the user to program the Master Clock (MCLK) and SPORT Serial Clock (SCLK), as with the AD73311, the AD73322 also allows the User to set the Sample Rate Divider...

- **DMCLK/2048 = Default Rate**
- **Selectable Rates of $MCLK \div N$; $N = 2048, 1024, 512$ and 256**

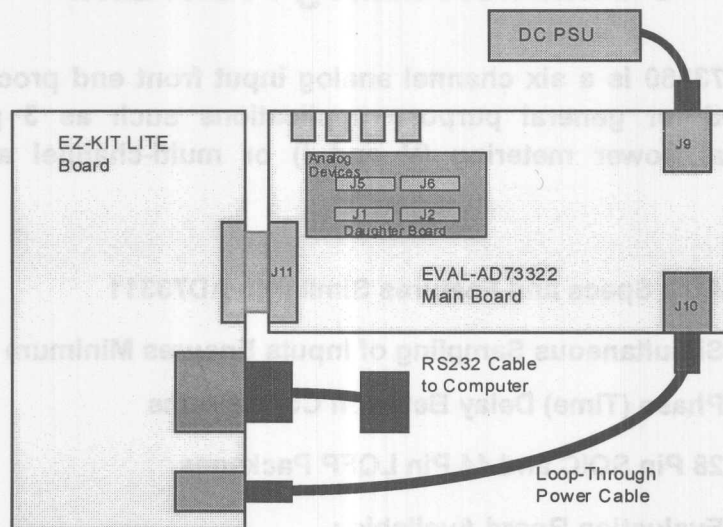


AD73322 Application : Wireless Local Loop (WLL)





AD73322 Evaluation Board



- Interfaces to ADSP-2181 EZKIT-Lite
- Up to 2 AD73322s in cascade - giving 4 I/O channels
- Cascade Length is selectable (2 or 4 I/O channels)



AD73360

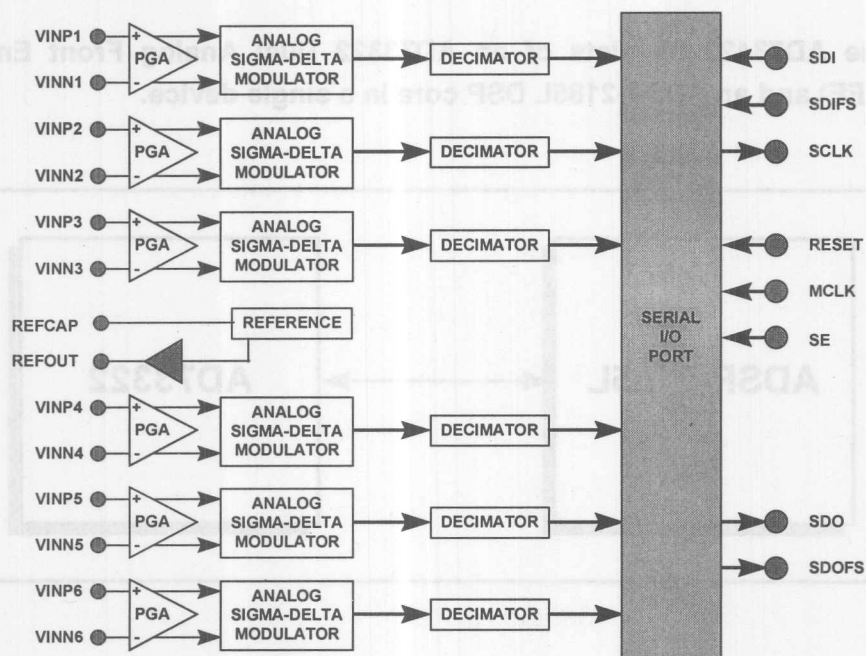
6 Channel Analog Front End

The AD73360 is a six channel analog input front end processor designed for general purpose applications such as 3 phase industrial power metering (V and I) or multi-channel analog inputs.

- **ADC Specs and Features Similar to AD73311**
- **Simultaneous Sampling of Inputs Ensures Minimum Phase (Time) Delay Between Conversions**
- **28 Pin SOIC and 44 Pin LQFP Packages**
- **Evaluation Board Available :**
 - **EVAL-AD73360EB**
 - **EVAL-AD73360EZ (EZ Kit Lite)**



AD73360 Block Diagram

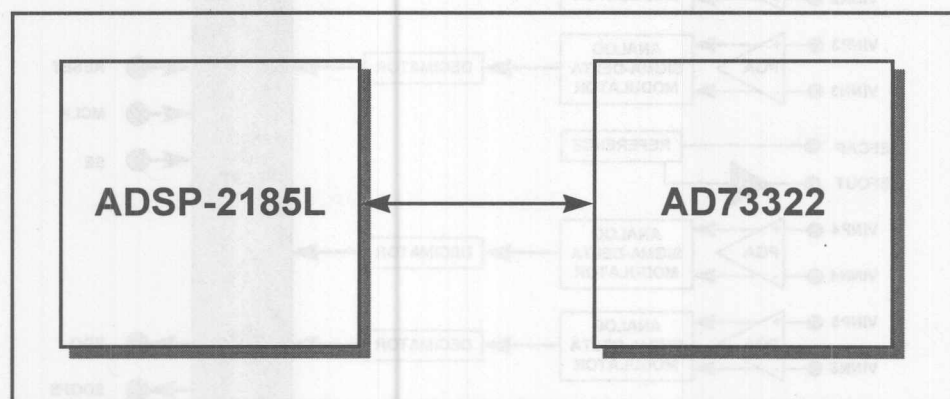




Preliminary
Information

AD73422 DSP Converter

The AD73422 consists of an AD73322 Dual Analog Front End (AFE) and an ADSP-2185L DSP core in a single device.





AD73342 Key Specs and Features

Basic AD73322 Specifications and Features, plus...

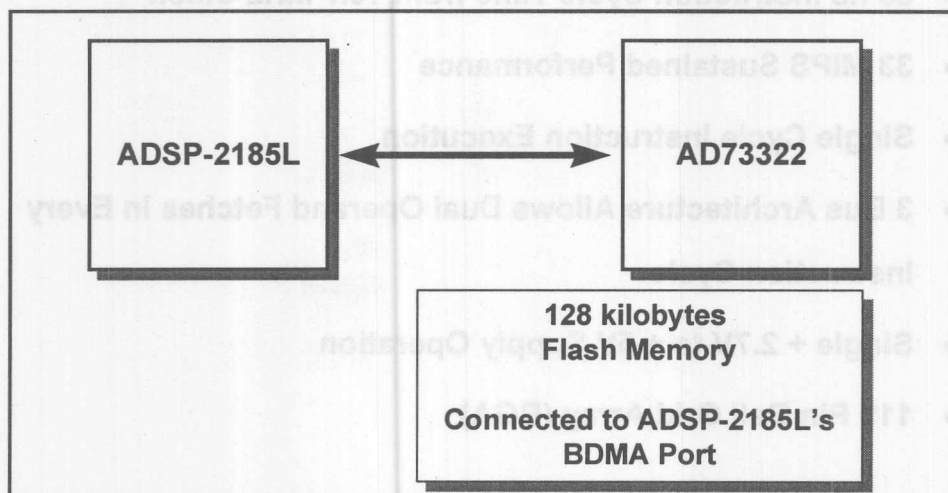
- 30 ns Instruction Cycle Time from 16.7 MHz Clock
- 33 MIPS Sustained Performance
- Single Cycle Instruction Execution
- 3 Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Single + 2.7V to + 5V Supply Operation
- 119 Pin Ball Grid Array (BGA)



**Preliminary
Information**

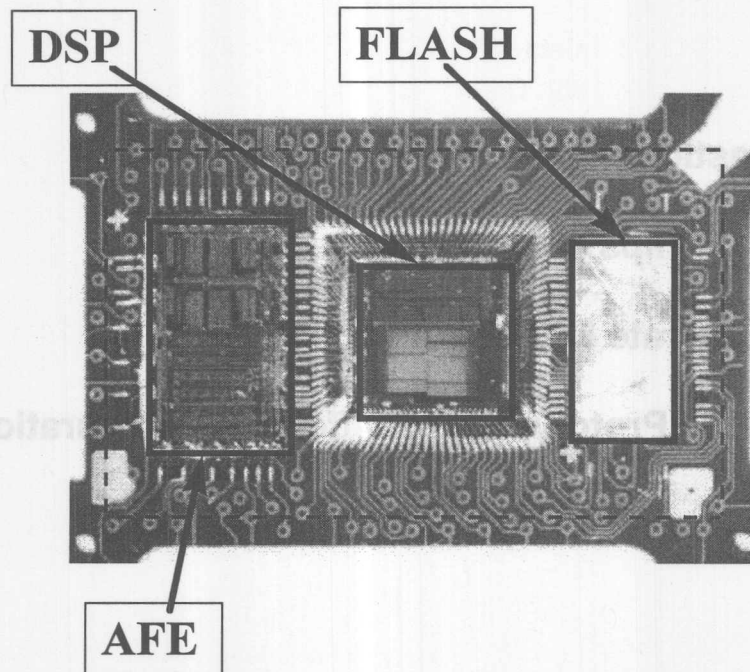
AD73522 DSP Converter

The AD73522 consists of an AD73322 Dual Analog Front End (AFE), an ADSP-2185L DSP core and on-board Flash Memory, all in a single device.





Plastic Ball Grid Array (PBGA)





Plastic Ball Grid Array (BGA)

- **Plastic Ball Grid Array (BGA)**
- **2(3) Chips Mounted on Substrate**
- **Substrate Is a Miniature PCB**
- **Rapid Prototyping of Different Configurations**



Generic Numbering Convention

AD733 x x x - xx

- DSP Memory Option
 - -40 : 2186 Equiv (40 kbytes)
 - -80 : 2185 Equiv (80 kbytes)
- Number of Output Channels
- Number of Input Channels
- 3 : AFE
- 4 : AFE & DSP
- 5 : AFE & DSP & Flash



Support Tools

DEVELOPMENT TOOLS :

- As the DSP Section Is a Standard Product It Is Fully Supported From the Present DSP 16-Bit Tools (Assembler, Linker/Loader, C Compiler, Simulator, ICE)

EVALUATION TOOLS :

- EZ Kit -Type Evaluation Tools are Currently Being Evaluated



Section 15

ADuC81X MicroConverter™ Series



MicroConverter™ Definition

High Performance Analog I/O

+

FLASH Memory

+

Microcontroller

=

MicroConverter™



Introducing the ADuC812

High Performance Analog I/O

12bit, 8ch ADC + dual 12bit DAC

+

FLASH Memory

8Kbyte Program + 640byte Data

+

Microcontroller

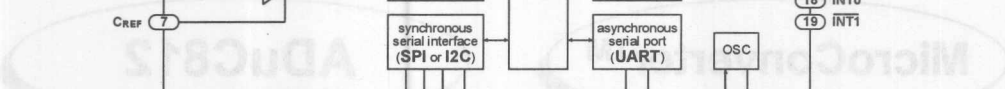
Industry Standard 8052

=

MicroConverter™

ADuC812

ADuC812





ADuC812 - Analog I/O

- **8 channel, 12bit, 5 μ s, Autocalibrating ADC**
 - **DMA Controller for High Speed Capture**
 - **True 12bit Performance (INL, SNR, etc.)**
- **Two 12bit, 4 μ s, Voltage Output DACs**
 - **Guaranteed 12bit Monotonicity**
- **On-Chip 2.5V Precision Bandgap Reference**
- **On-Chip Temperature Sensor**
- **Simple ADC & DAC Control Through Software or Hardware**



ADuC812 - FLASH Memory

- **RETAIN DATA WITHOUT POWER!**
- **8Kbytes Nonvolatile Program Memory (“read only”)**
 - Stores Program and Fixed Lookup Tables
 - In-Circuit Serial Programmable or External Parallel Programmable
- **640 bytes Nonvolatile Data Memory (“read/write”)**
 - User “Scratch Pad” for Storing Data During Program Execution
 - Simple Read/Write Access Through SFR Space
- **Built-In Security Features for Both Program & Data FLASH**
- **Programming Voltage (V_{pp}) Generated On-Chip**



ADuC812 - Microcontroller

- **Industry Standard 8052 Core**
 - **12 Clock Machine Cycle w/ up to 16MHz Clock**
 - **32 Digital I/O Pins**
 - **Three 16 bit Counter/Timers**
 - **UART Serial Port**
- **...Plus Some Useful Extras**
 - **SPI or I²C Compatible Serial Interface**
 - **WatchDog Timer**
 - **Power Supply Monitor**

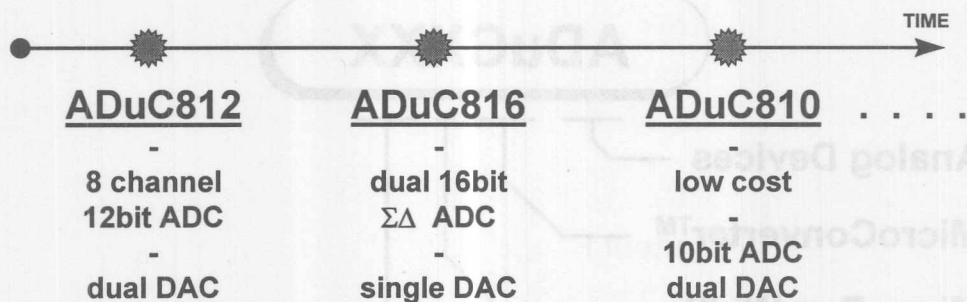


ADuC812 - Primary Specifications

- **ADC**
 - INL $\pm\frac{1}{2}\text{LSB}$
 - SNR 70dB
 - Input Range 0 to V_{REF}
 - Conv. Time $5\mu\text{s}$
- **DAC**
 - DNL $\pm\frac{1}{2}\text{LSB}$
 - Output Range 0 to V_{REF} -or- 0 to V_{DD}
 - Settling Time $4\mu\text{s}$
- **Power**
 - Specified for 3V or 5V Operation
 - | | <u>5V</u> | <u>3V</u> |
|-----------|-----------------|-----------------|
| Normal | 18mA | 12mA |
| Idle | 10mA | 6mA |
| Powerdown | $50\mu\text{A}$ | $50\mu\text{A}$ |



MicroConverter™ Product Roadmap

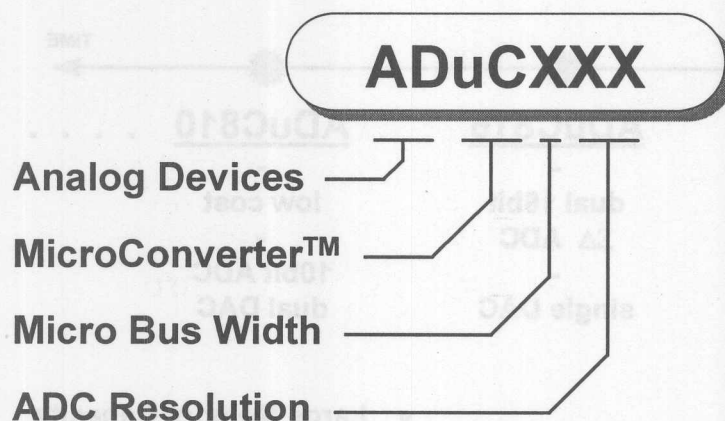


.... Future Products May Include:

- Large Memory Capacity
- Hardware Communications Interface Enhancements
- Increased Microcontroller Horsepower



MicroConverter™ - Part Numbering Scheme



Eg: **ADuC812 ; ADuC816 ; ADuC810**



MicroConverter™ - Typical Applications

- **Sensors and Remote Signal Sources**
- **Portable Instrumentation**
- **Data Loggers**
- **Battery / Supply Monitoring and Management**
- **Medical Instruments**
- **Appliances**
- **Etc....**

Wherever Digitally Programmable Analog I/O is Useful!



MicroConverter™ - Development Tools

Assembler : Metalink 2-Pass Assembler

Simulator : Windows Based Full-Function Simulator

Serial Downloader : For In-Circuit Programming

Debugger : Windows Based Serial Port Debugger

**Emulator : Metalink Windows Emulation Tools to
Fully Support the MicroConverter™
Product Line. Metalink's Proprietary
'Enhanced Hooks' Emulation Scheme is
Designed onto Silicon.**



MicroConverter™ - QuickStart™ Development Kit

- **Documentation**
 - Datasheet
 - User's Guide
 - Quick Reference Guide
 - Development Kit Document
- **Evaluation Board**
 - Serial Comms
 - 32K External SRAM
 - Buffered Analog I/O
- **Regulated Power Supply**
- **Serial Port Cable**
- **Software**
 - Assembler
 - Simulator
 - Serial Downloader
 - Debugger
 - Example Code



QuickStart™ Development Kit MicroConverter™

- Documentation
 - Datasheet
 - User's Guide
 - Quick Reference Guide
 - Development Kit Document
- Evaluation Board
 - Serial Comm
 - 32K External SRAM
 - Buffered Analog I/O
- Software
 - Assembler
 - Stimulator
 - Serial Downloader
 - Debugger
 - Example Code
- Regulated Power Supply
- Serial Port Cable



Section 16

PLL Frequency Synthesizers



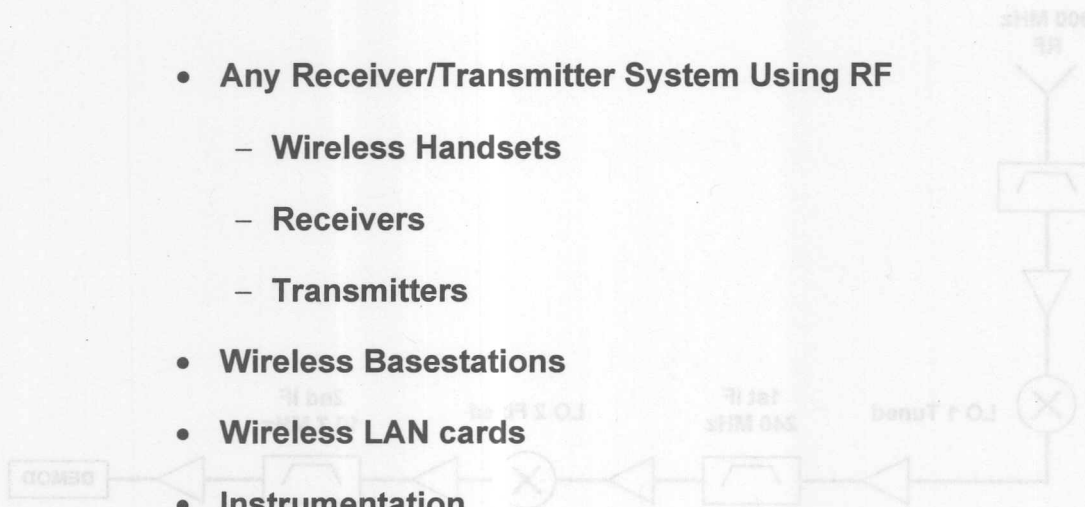
PLL - Phase Locked Loop

**VCO - Voltage Controlled
Oscillator**



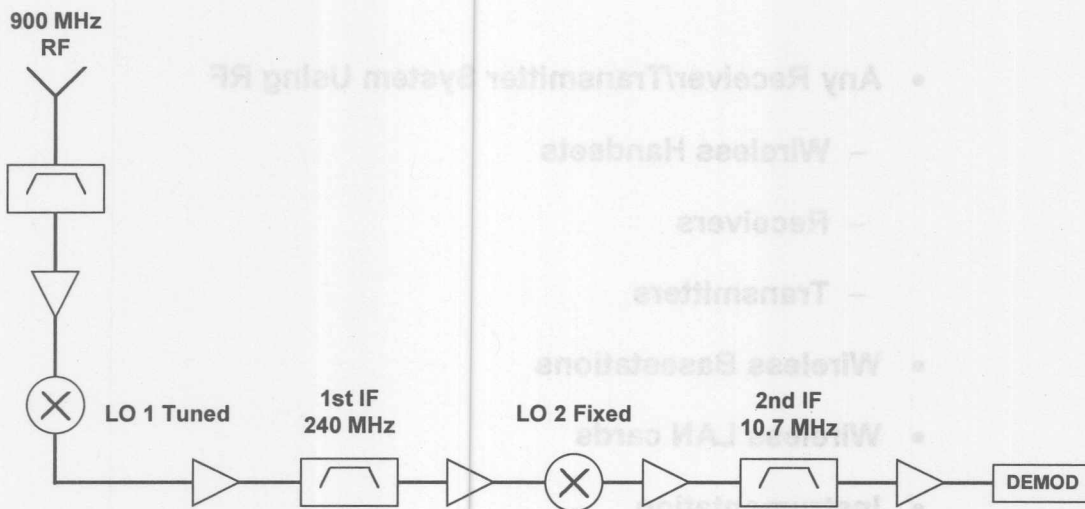
Where Are PLLs/VCOs Used ?

- Any Receiver/Transmitter System Using RF
 - Wireless Handsets
 - Receivers
 - Transmitters
- Wireless Basestations
- Wireless LAN cards
- Instrumentation





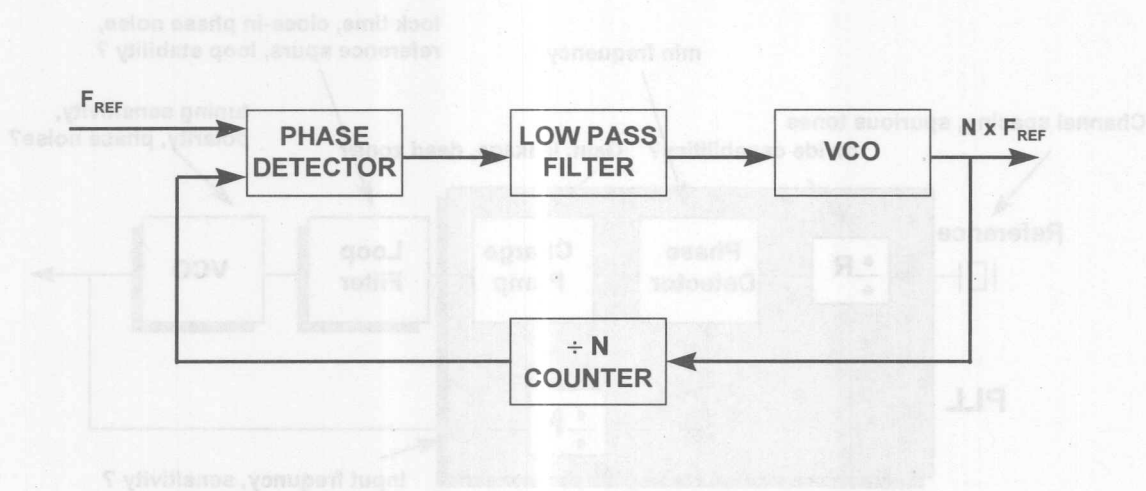
Where Are PLLs/VCOs Used ?



Dual Conversion Superheterodyne Receiver

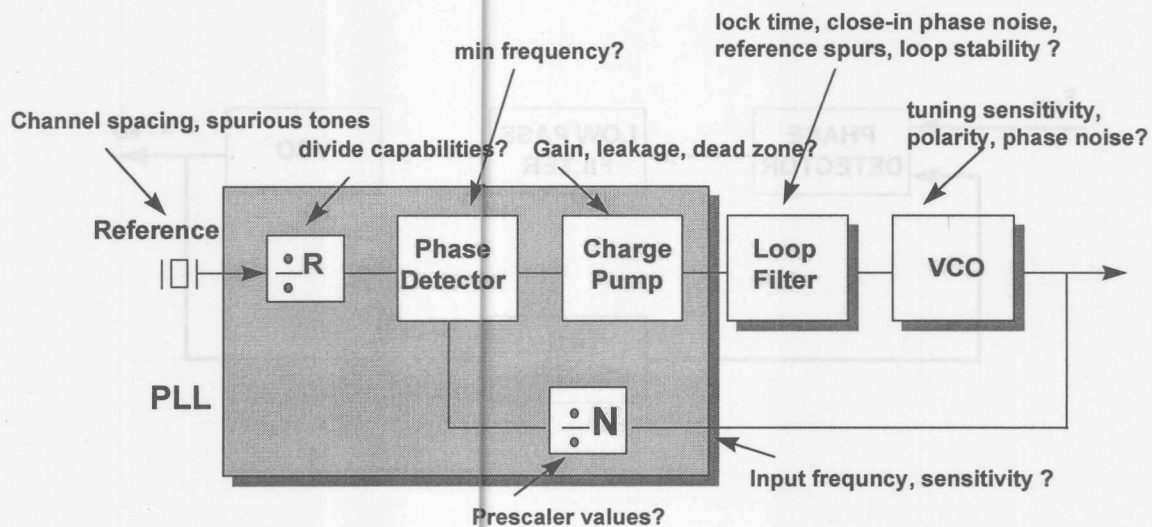


Basic PLL System



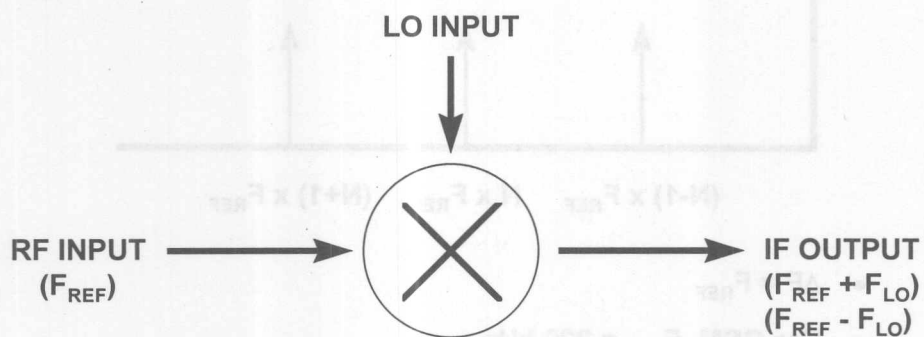


PLL Performance Issues





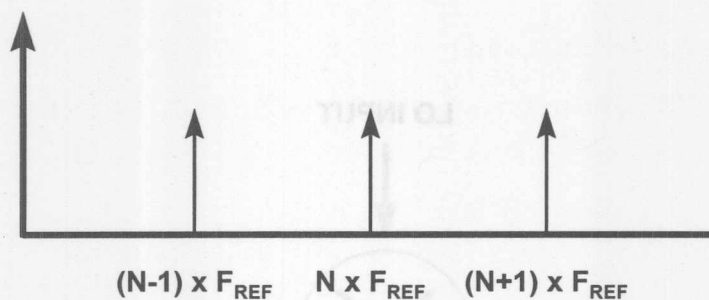
What is a Mixer ?



The Ideal Mixer



Channel Spacing for Integer N PLL



- $\Delta F = F_{REF}$
- For GSM, $F_{REF} = 200$ kHz
- $F_{RF} = 925$ MHz to 960 MHz for the Receiver
- If First IF is set at 240 MHz then LO Must Go From 685 MHz to 720 MHz
- This Means N Must Vary From 3425 to 3600

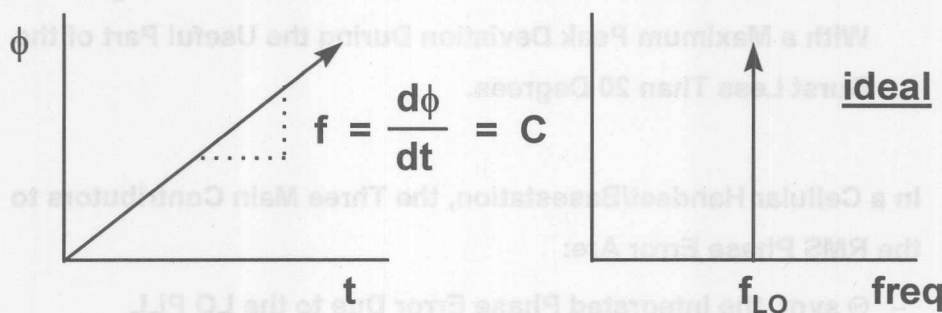


Effects of Phase Noise On Cellular Systems

- **GSM Phase Accuracy Specification:**
 - **The RMS Phase Error Shall Not Be Greater Than 5 Degrees With a Maximum Peak Deviation During the Useful Part of the Burst Less Than 20 Degrees.**
- **In a Cellular Handset/Basestation, the Three Main Contributors to the RMS Phase Error Are:**
 - **⊕ synt, the Integrated Phase Error Due to the LO PLL Synthesizer**
 - **⊕ baseband, the Integrated Phase Error Due to the Baseband Converter**
 - **⊕ (I&Q), the Integrated Phase Error Due to the IQ Modulator**



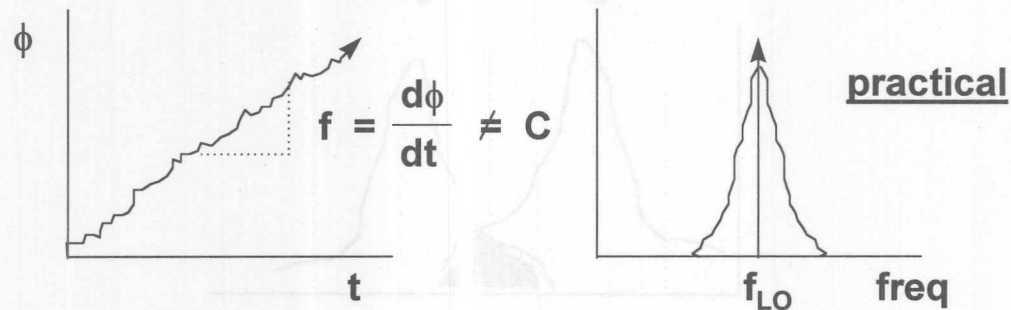
Phase Noise



An Oscillator Frequency Is Equal to the Time Derivative of Phase.
Constant Oscillator Phase Slope Equates to Unique Frequency in
the Frequency Domain.



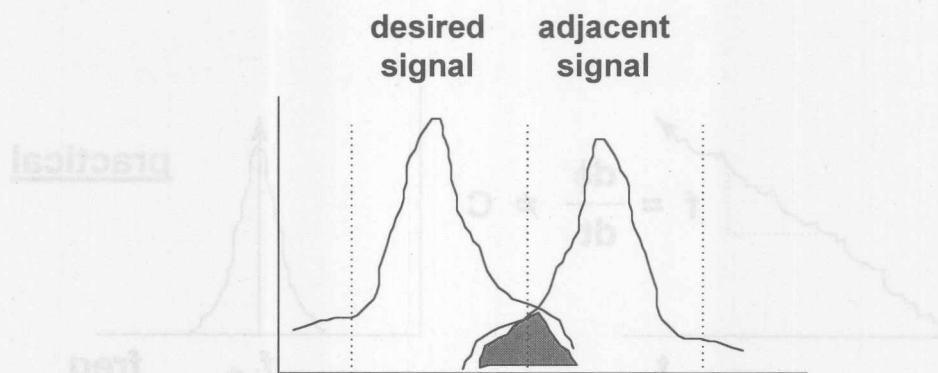
Phase Noise



In Practice, Oscillator Noise Exists on the Phase Slope (Phase Noise) An Oscillator Frequency Spectrum “Spreads” in the Presence of Phase Noise.



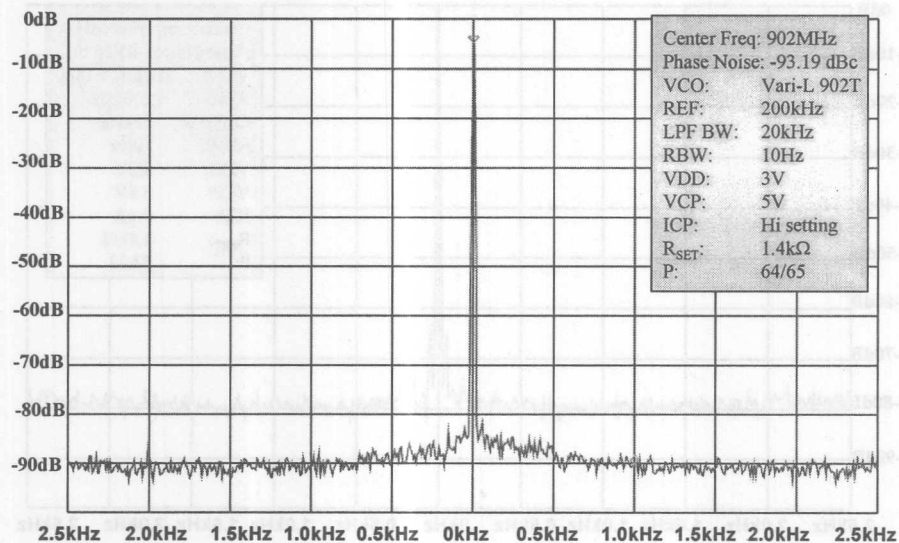
Phase Noise



Signal Desensitization Is a Natural Result of Frequency Translation With Practical Oscillators Due to Adjacent Channel "Frequency Spreading", Amplification Causes Spectral "Growth".

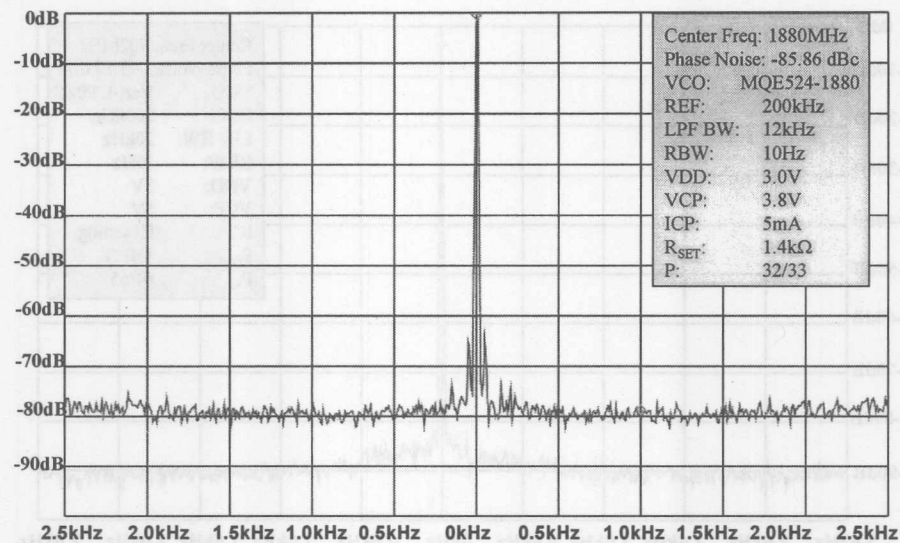


GSM - Phase Noise



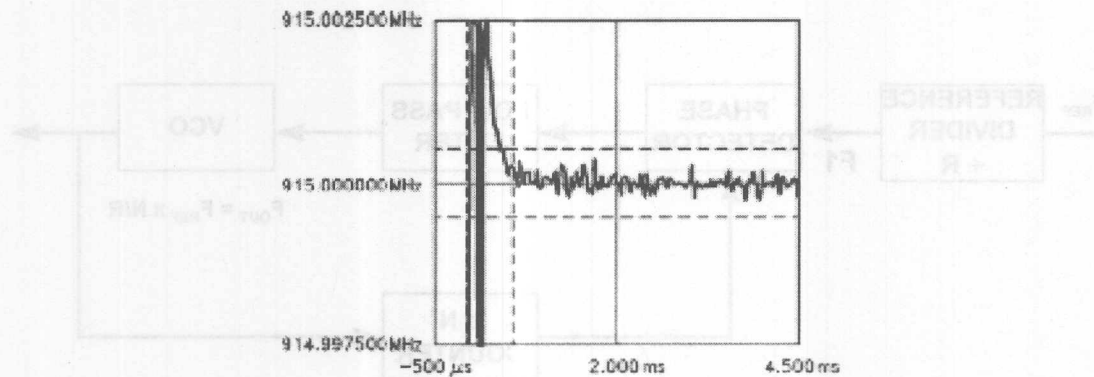


DCS GSM - Phase Noise





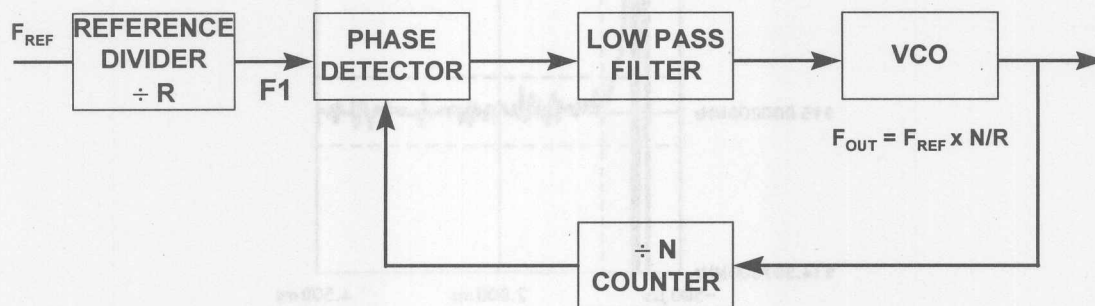
Lock Time



Settling Time Is Proportional to F_{REF} and the Loop Bandwidth



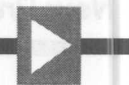
Using a Reference Divider



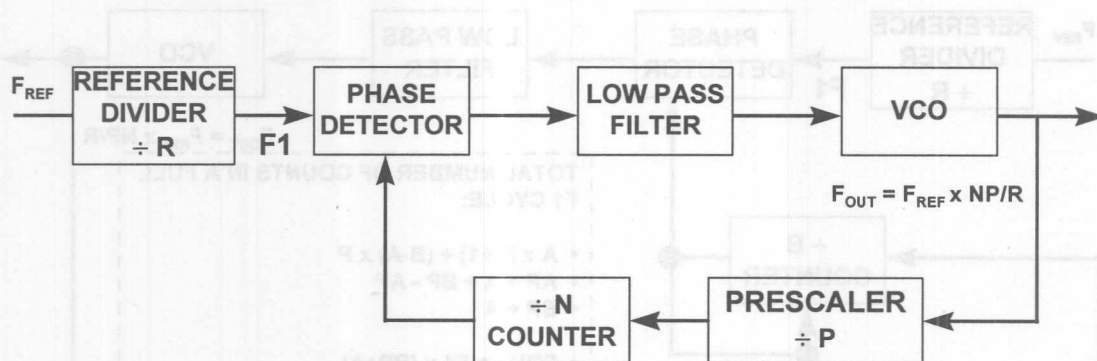
$$F_{OUT} = F_1 \times N$$

$$F_{OUT} = (F_{REF}/R) \times N$$

$$F_{OUT} = F_{REF} \times (N/R)$$



Prescaler



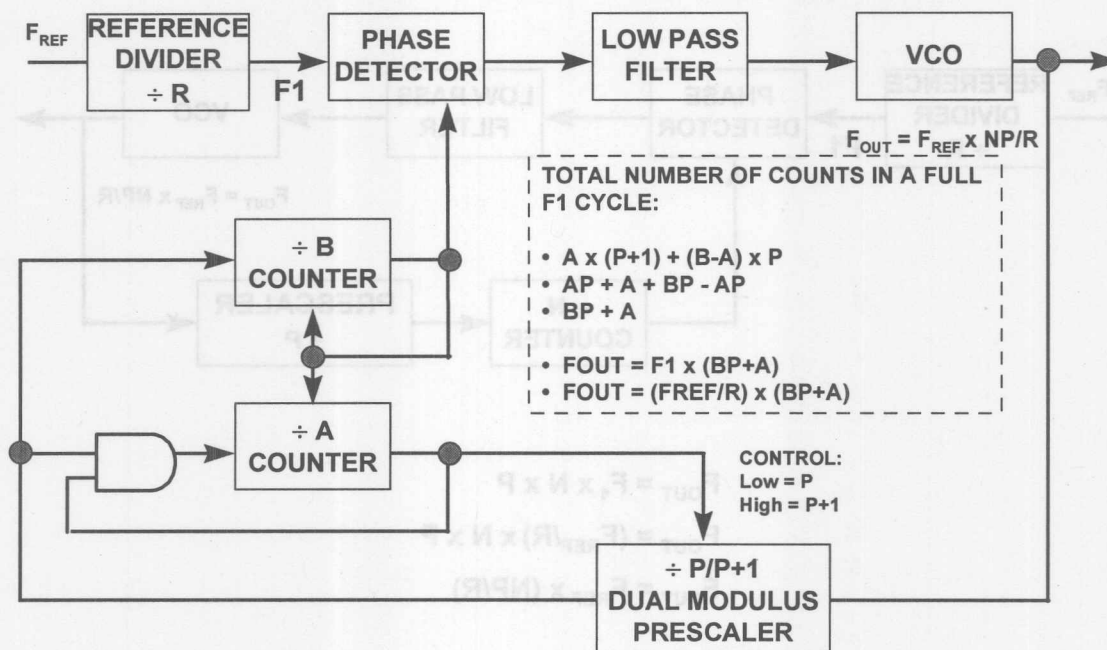
$$F_{OUT} = F_1 \times N \times P$$

$$F_{OUT} = (F_{REF}/R) \times N \times P$$

$$F_{OUT} = F_{REF} \times (NP/R)$$

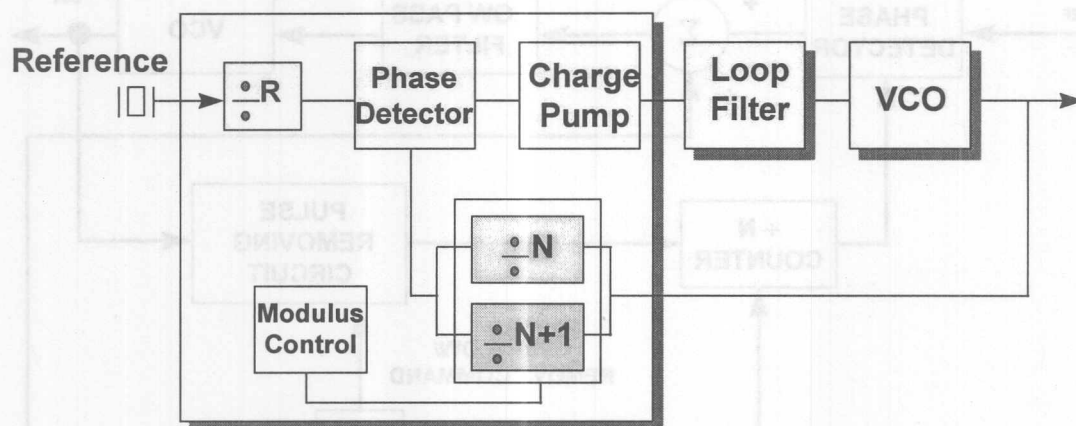


Dual Modulus Prescaler





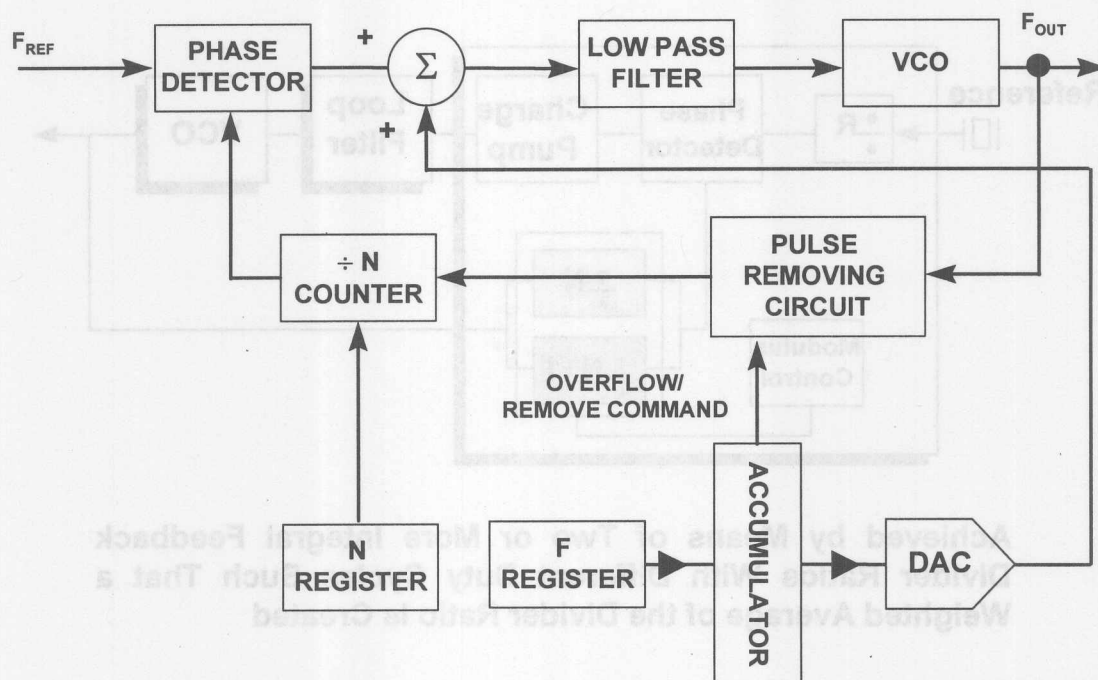
Fractional-N PLL



Achieved by Means of Two or More Integral Feedback Divider Ratios With Different Duty Cycles Such That a Weighted Average of the Divider Ratio Is Created

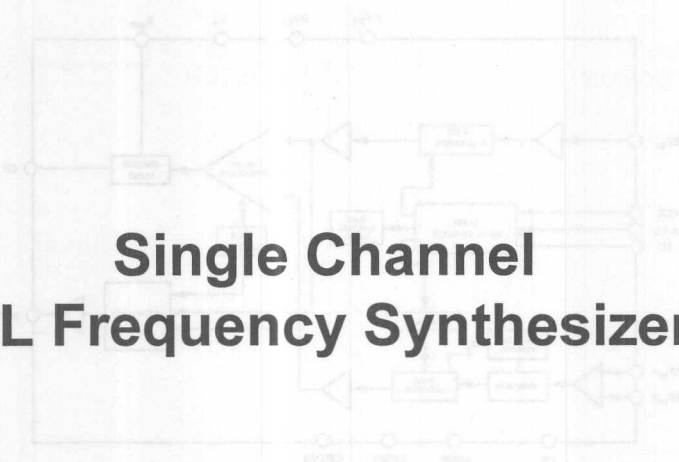


Fractional-N PLL





Single Channel PLL Frequency Synthesizers

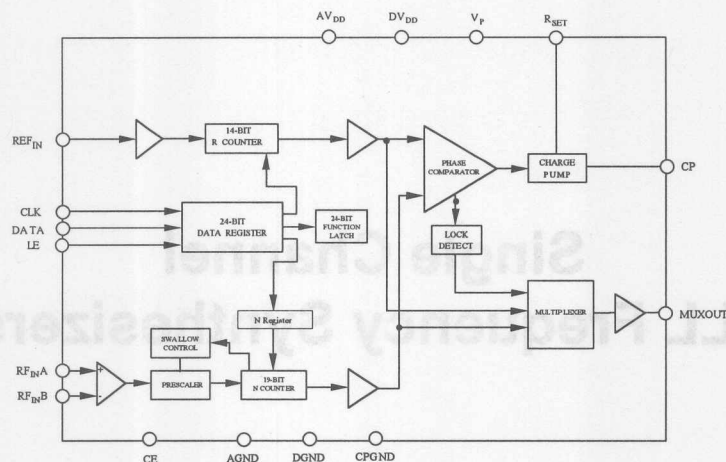


The ADP4110/ADP4112 are frequency synthesizers which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They use a digital phase locked loop technique which, when combined with a bit duality reference and a loop filter, results in a stable, low-noise signal for the VCO.



ADF4110 - ADF4112

Single PLL Frequency Synthesizers



The ADF4110/ADF4111/ADF4112 are frequency synthesizers which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They use a digital phase locked loop technique which, when combined with a high quality reference and a loop filter, results in a stable, low-noise signal for the VCO.



ADF4110 - ADF4112 : Key Specs and Features

- **RF Input Frequencies (min/max) :**
 - ADF4110 : 25/550 MHz
 - ADF4111 : 0.1/1.2 GHz
 - ADF4112 : 0.1/3.0 GHz
- **Reference Input Frequency : 5/40 MHz, min/max**
- **Phase Detector Frequency : 10 MHz max**
- **Phase Noise Floor : -155 dBc/Hz, typ**
- **Software Programmable Dual Modulus Prescaler:**
 - 8/9, 16/17, 32/33, 64/65



ADF4110 - ADF4112 : Key Specs and Features

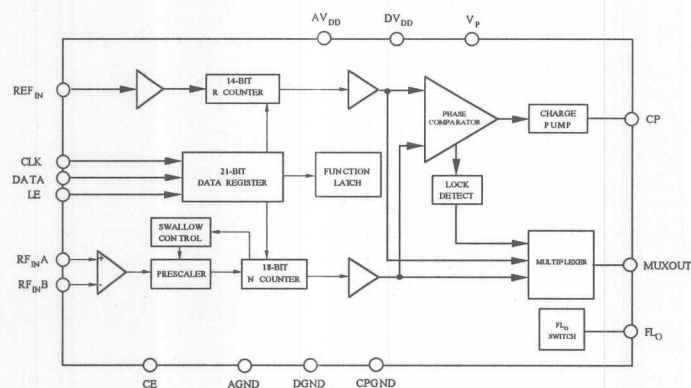
- **Programmable Charge Pump Currents**
 - 625 uA - 5 mA, typ
- **Programmable Anti-Backlash Pulse Width**
- **3-Wire Serial Interface**
- **Digital Lock Detect**
- **+2.7 V to +5.5 V Power Supply**
- **Power Down Mode : 1 uA, typ**
- **16 Pin TSSOP Package**



ADF4116 - ADF4118

Single PLL Frequency Synthesizers

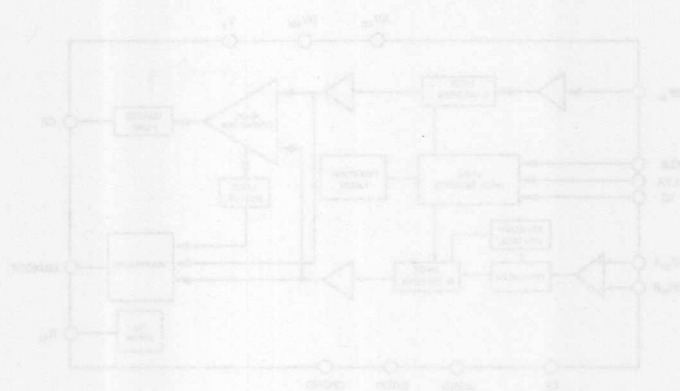
The ADF4116-ADF4118 offer the same features as the ADF4110-ADF4112 except the pre-modulus prescaler and charge pump current are not programmable





ADP4116 - ADP4118 Single PLL Frequency Synthesizers

The ADP4116-ADP4118 offer the same features as the ADP4110-ADP4112 except the pre-modulus prescaler and charge pump current are not programmable.





Fractional - N PLL Frequency Synthesizers

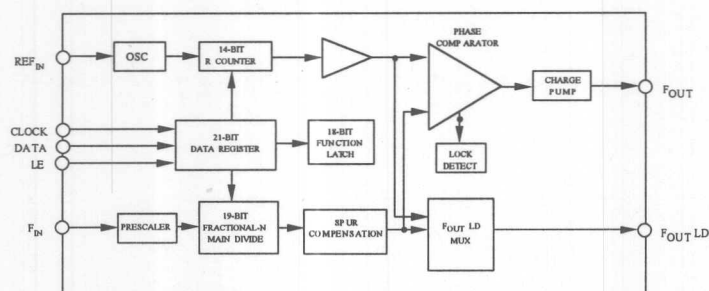


Fractional-N PLL

- **Advantage of Fractional-N :**
 - **Reference Can Be Multiple Times the Channel Spacing (Smaller N)**
 - **Loop Filter Bandwidth Can Be Increased (Faster Lock Time)**
- **Problems :**
 - **Multiple Divide Ratios Create Fractional Spurs**
- **Several Methods of Dealing With Fractional Spurs :**
 - **Spur Compensation**
 - **Noise Shaping**
 - **Combination of Both**



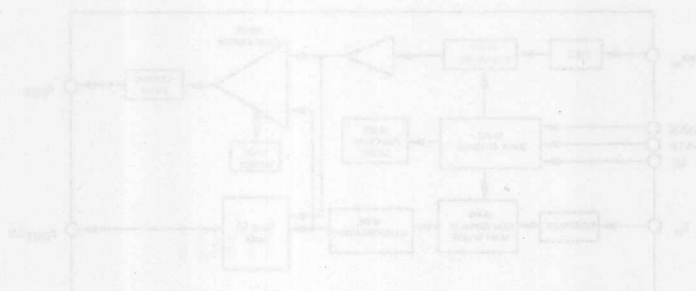
ADF4150 - ADF4152 Fractional-N PLL Synthesizers



- RF Input Frequencies (min/max) :
 - ADF4110 : 25/550 MHz
 - ADF4111 : 0.1/1.2 GHz
 - ADF4112 : 0.1/3.0 GHz
- Modulo-32 Fractional-N Main Counter (fractional denominators of 2,4,8,16 &32)
- 20-pin TSSOP package



ADF4150 - ADF4152 Fractional-N PLL Synthesizers



• RF Input Frequencies (minimum):

- ADF4150 : 25/500 MHz
- ADF4151 : 0.012 GHz
- ADF4152 : 0.012 GHz

• Modulo-32 Fractional-N Main Counter (fractional denominator of 2,4,8,16,32)

• 20-pin TSSOP package



Dual Channel PLL Frequency Synthesizers



ADF4206 - ADF4208 Dual PLL Frequency Synthesizers

- **RF Input Frequencies (min/max) :**
 - ADF4206 : 0.1/1.2 GHz
 - ADF4207 : 0.1/2.0 GHz
 - ADF4208 : 0.1/2.5 GHz
- **Reference Input Frequency : 5/40 MHz, min/max**
- **Phase Detector Frequency : 10 MHz max**
- **Phase Noise Floor : -155 dBc/Hz, typ**
- **Selectable Dual Modulus Prescaler and Charge Pump Currents**
- **Complimentary PreScaler Inputs (ADF4207)**



ADF4206 - ADF4208 : Key Specs and Features

- **3-Wire Serial Interface**
- **Digital Lock Detect**
- **+2.7 V to +5.5 V Power Supply**
- **Power Down Mode : 1 uA, typ**
- **Package Styles :**
 - **ADF4206, ADF4208 : 16 Pin TSSOP**
 - **ADF4207 : 20 Pin TSSOP**



ADP4306 - ADP4308 : Key Specs and Features

- 3-Wire Serial Interface
- Digital Lock Detect
- +2.7 V to +6.5 V Power Supply
- Power Down Mode : 1 nA typ
- Package Styles :

- ADP4306, ADP4308 : 16 Pin TSOP

- ADP4307 : 20 Pin TSOP